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Feedforward Active Substrate Noise Cancelling Based on di/dt of Power Supply

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SUMMARY This paper demonstrates a feedforward active substrate noise cancelling technique using a power supply di/dt detector. Since the substrate is usually tied with the ground line with a low impedance, the substrate noise is closely related to the ground bounce which is proportional to the di/dt when inductance is dominant on the ground line impedance. Our active cancelling detects the di/dt of the power supply, and injects an anti-phase current into the substrate so that the di/dt-proportional substrate noise is cancelled out. Our first trial shows that 34% substrate noise reduction is achieved on our test circuit, and the theoretical analysis shows that the optimized canceller design will enhance the substrate noise suppression ratio up to 56%.

key words: *substrate noise, di/dt, feedforward active cancelling, anti-phase, ground bounce, di/dt detector*

1. Introduction

As the growing demand of analog-digital mixed signal LSIs such as A/D, D/A and PLLs integrated with large scale digital circuits, substrate noise becomes serious concern. Although power lines for digital and analog circuits are isolated in order to prevent the coupling of the digital switching noise to the analog circuits, the digital noise is transferred to the analog blocks via the common substrate.

Noise on a power line is caused by di/dt noise and resistive voltage drop due to the parasitic impedance of the power line. As the operating frequency of LSIs becomes higher, the $L(di/dt)$ noise is becoming dominant compared with the IR drop. Typically, the digital ground line is connected to the substrate in every CMOS gate, which results in a very low resistance between the digital ground line and the substrate. Hence the digital ground noise and ringing will also be present on the substrate. One report shows that the substrate noise has the same shape with 1/8 amplitude of the ground noise [1].

Guard rings are widely used to suppress the substrate noise. However, the parasitic impedance of the guard line degrades the efficiency of the noise absorption especially for high frequency noise [2]. Also it is sometimes difficult to provide a clean ground source, and a guard ring terminated to a noisy ground is possible to inject the substrate noise instead of noise reduction.

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A feedforward active guard band is another technique for the substrate noise reduction, in which the substrate noise is detected and the anti-phase noise signal is actively supplied to the guard band [2], [3]. This technique uses a differential amplifier to sense the original substrate noise and generates the anti-phase noise signal, however, the frequency response and the delay of the amplifier restricts the noise cancelling bandwidth, in addition that the original substrate noise voltage is too small to generate the anti-phase signal with enough amplitude. And feedback systems are sometimes unstable in some frequency range.

This paper demonstrates a feedforward active substrate noise cancelling technique using a power supply di/dt detector [4].

2. Circuit Design

2.1 Feedforward Active Substrate Noise Cancelling

The main cause of substrate noise is a coupling from digital power lines since the substrate and the digital ground are connected with a low impedance for stabilizing the body voltage of NMOS. The ground noise is caused by the supply current and the ground line impedance. As the LSI operating frequency becomes higher, the $L(di/dt)$ noise is becoming dominant over the IR drop, thus the ground noise amplitude is proportional to the di/dt. Therefore, the substrate noise is also proportional to the di/dt. Thus a di/dt detector [5], [6] can be applicable for cancelling the di/dt-proportional substrate noise.

A block diagram of our feedforward active substrate noise cancelling system is shown in Fig. 1. The ground

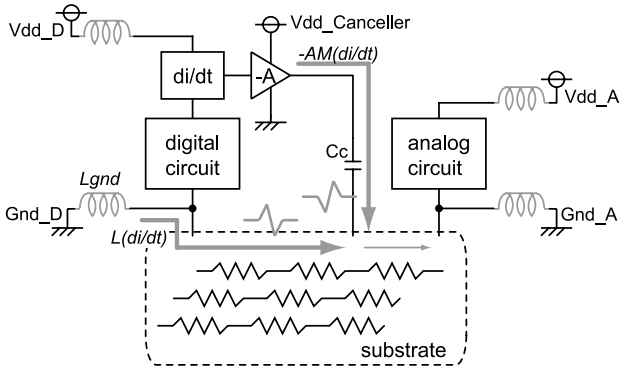

Fig. 1 Feedforward active substrate noise cancelling.

noise is caused by the power supply di/dt and L_{gnd}. The di/dt-proportional ground noise is transferred to the analog circuit through the substrate resistance. Here, the p-sub/Nwell junction capacitor is negligibly small compared with the ground line-substrate impedance that the Vdd_D bounce is not transferred to the substrate. On the other hand, the di/dt detector on the power line generates the di/dt-proportional voltage, and the following amplifier can generate minus di/dt signal which has anti-phase against the substrate noise. By injecting the anti-phase signal into the substrate, the substrate noise can be cancelled out.

The advantage of this structure is that there is no feedback loop which leads stable and high-bandwidth noise cancelling. Another advantage is that the di/dt detector can generate larger induced voltage on the terminals than the substrate noise voltage that the gain of the amplifier can be small compared with the active guard band technique [3].

2.2 di/dt Detector and Noise Canceller

The substrate noise canceller is basically the same as the di/dt detector [5], [6], where a mutual inductor coupled to the power supply line induces the di/dt-proportional voltage, and an following amplifier generates minus di/dt-proportional signal which has anti-phase against the substrate noise, as shown in Fig. 2.

Since the substrate is tied to the ground voltage, the coupling capacitor C_c is inserted at the output of the amplifier to prevent the bias voltage change of the node $n2$. Here, the input impedance of the substrate from the injection point is assumed to be pure resistive. In order to inject the current with the appropriate phase, the impedance of the coupling capacitor C_c should be small enough compared with the substrate resistance for the target noise frequency range. The substrate resistance is relatively small, the gain of the amplifier is small and the cut-off frequency can get higher. Therefore, the amplifier can be considered as a voltage controlled current source, and the injected current has the same phase as $-V2$ which has the anti-phase against the di/dt.

2.3 Substrate Noise Probing for Verification

The substrate noise probing circuit implemented for verification purpose is shown in Fig. 3. The noise is probed using an differential amplifier at the first stage with one input connected to the substrate and the other to an external ground as a reference. The input terminals are biased as half-Vdd by the resistors R_b, where the amplifier has the maximum gain. The resistance is large enough to be considered as open for AC signals. Since the substrate voltage is around ground voltage, the coupling capacitors C_c are used here as well.

Since substrate contacts of NMOS may disturb the original substrate noise waveform, the body terminals of MN1 in the amplifier are not tied even though it may lead to an unstable amplifier operation. The second and third stage amplifiers are composed of PMOS and resistors and the final stage is a PMOS open drain structure without using NMOS for eliminating the substrate contacts. Here, the ratio of $\Delta I_d/\Delta V_g$ and $\Delta I_d/\Delta V_{bs}$, which is g_m/g_{bs}, is 6.0 on NMOS according to HSPICE simulation. Thus, the amplifier has enough gain even though the noise voltage for the gate and the substrate are the same.

2.4 Internal Circuit as Noise Source

Figure 4 shows our internal circuit as a noise generator. The test circuit contains VCO so that we can easily sweep the operating frequency by changing the DC control voltage ($Vctrl$). The frequency divider generates 101010... signal for the input to the shift resister. The SEL circuit can select

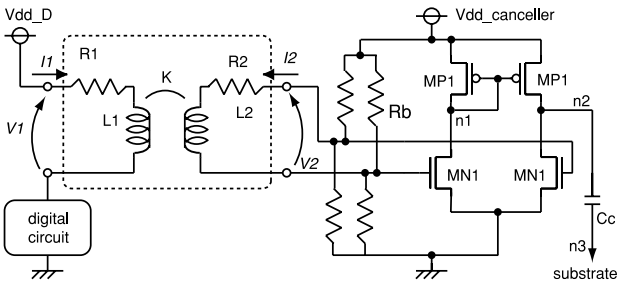

Fig. 2 The di/dt detector and noise canceller.

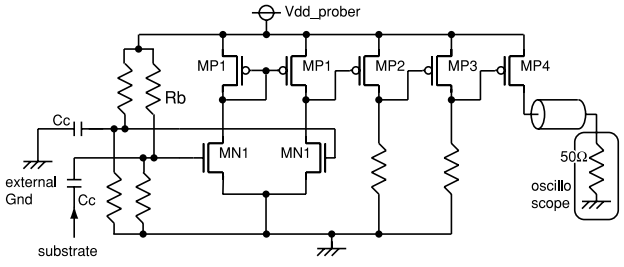

Fig. 3 Substrate noise prober.

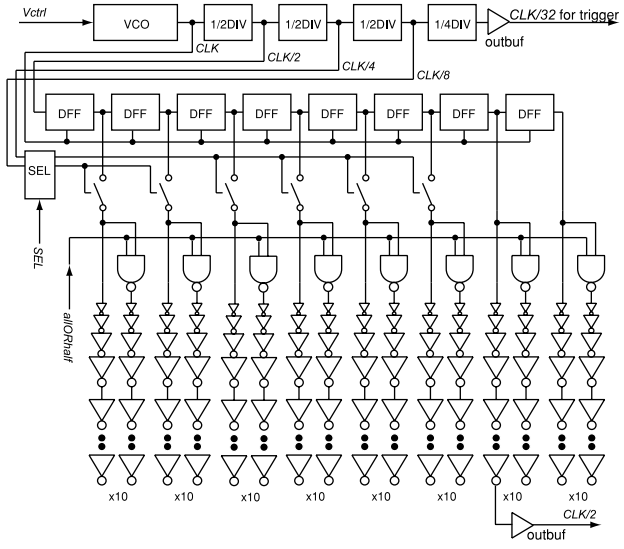

Fig. 4 Internal circuit as a noise source.

the operating mode, a repeat mode or a random mode. On the repeat mode, the SEL circuit always outputs "High" signal, the signal change from the DFFs are transferred to the inverter chains and the circuit consumes the same amount of current at every clock cycle. On the random mode, the SEL circuit passes $CLK/4$, $CLK/8$ signals, the DFF outputs and some inverter chains are disconnected when the SEL outputs are "Low," and hence the current waveform becomes different in accordance with the divided clock signals. $allORhalf$ signal controls the activation ratio of the circuit. This circuit represents common synchronous circuits operating on CLK. The $CLK/32$ output is used as a trigger for a oscilloscope, and the $CLK/2$ output is used as a reference for the timing consideration.

2.5 Design Parameters

The circuit is designed using 0.35 μm 3-ML 2-Poly standard CMOS technology. The mutual inductor of the di/dt detector consists of the power supply line and an underlying spiral inductor. The power supply line L_1 is composed of the top metal layer ML3 with 1 turn, 20 μm width. The spiral inductor L_2 has 24 turns with 2 μm width and 2 μm spacing using ML1. The outside diameter of the both inductors are 200 μm $\times$ 200 μm. The equivalent circuit of this mutual inductor structure is extracted by FastHenry [7] 3D field solver. The coupling capacitor C_c is formed using poly-poly capacitor, and the designed value is about 25 pF. The bias resistor R_b is formed using gate-poly without silicide and the designed value is about 10 kΩ. The necessary parameter values are listed in Table 1.

Table 1 Designed parameter value.

mutual inductor	L_1	L_2	K	R_1	R_2
	0.86 nH	53.3 nH	0.603	2.3 Ω	218 Ω
amp for canceller	W_{pmos}	W_{nmos}	R_b	C_c	
	200 μm	100 μm	10 kΩ	25 pF	
amp for prober	W_{pmos1}	W_{nmos1}	R_b	C_c	W_{pmos4}
	20 μm	10 μm	10 kΩ	25 pF	160 μm

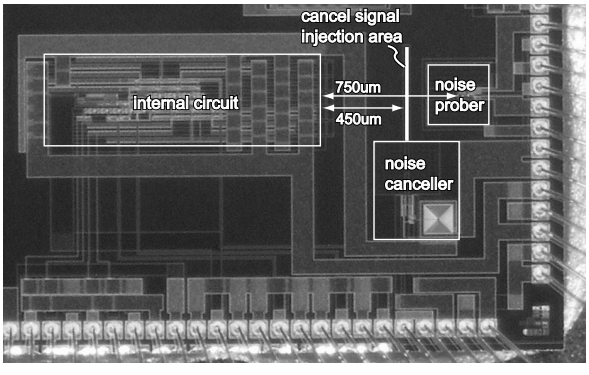

Fig. 5 Chip photograph of the feedforward active noise cancelling circuit, using 0.35 μm CMOS process. The area is 3.0 mm $\times$ 1.8 mm.

2.6 Floorplan

Figure 5 shows a chip photograph of our test circuit. The chip area is 3.0 mm $\times$ 1.8 mm.

The substrate noise probing point is located 750 μm apart from the noise source with the size of 20 μm $\times$ 50 μm P^+ active region, and the cancel signal injection area is located between the noise source and the probing point with the size of 10 μm $\times$ 580 μm P^+ active region on P^- substrate.

3. Measurement

3.1 Setups

In order to measure high-speed noise waveforms, the chip is mounted on a Cu board as shown in Fig. 6. All the inputs including $Vdd\_internal$, Vdd_io, $Vdd\_canceller$, Vdd_prober, $Vctrl$, SEL and $allORhalf$ are DC and supplied through lead lines to the "islands" on the board. The voltage of the islands are stabilized by several chip capacitors. 50 Ω transmission lines are directly connected to the high-speed output pins including $CLK/2$, $CLK/32$ and the substrate noise prober output, in order to reduce reflections.

3.2 Substrate Noise Waveforms

The measured waveforms of the substrate noise and the $CLK/2$ signals are shown in Fig. 7. The active cancel OFF and ON means that $Vdd\_canceller$=0 V for OFF state where the noise canceller injects no signal into the substrate and the original substrate noise is probed, while $Vdd\_canceller$=3.3 V for ON state where the cancel signal suppresses the substrate noise. Figure 7(a) is on the repeat mode, and Fig. 7(b) is on the random mode. The operating frequency is 500 MHz, and the gain of the noise prober at this frequency is about 7.5 by HSPICE simulation. The prober output has about 1 V bias because the on-resistance of the final stage PMOS of the prober circuit is about 100 Ω, as shown in Fig. 3. The graphs show that our feedforward

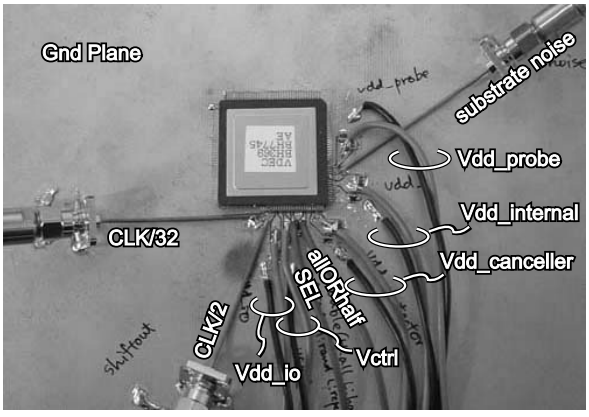

Fig. 6 Photograph of the chip mount.

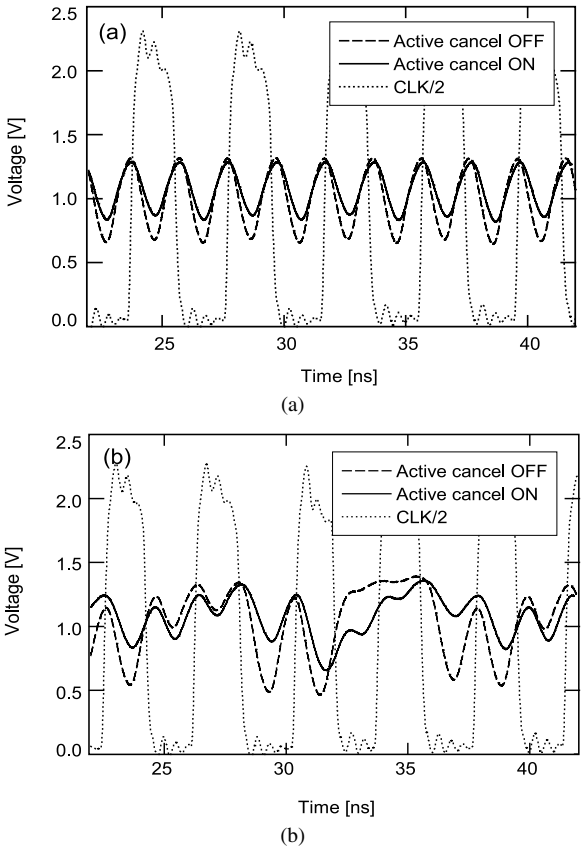

Fig. 7 Substrate noise waveforms with the active noise cancelling ON/OFF, together with the $CLK/2$ signal. The operating frequency is 500 MHz. (a) Repeat mode, and (b) Random mode.

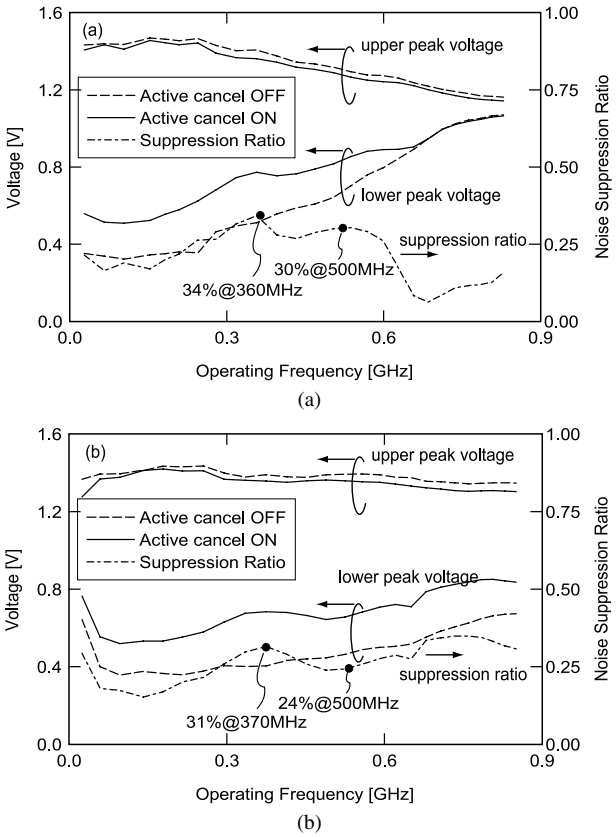

Fig. 8 The frequency dependence of the upper and lower peaks of the substrate noise voltage, together with its suppression ratio by the feedforward active noise cancelling (a) on the repeat mode, (b) on the random mode.

active cancelling circuit cancels and reduces the substrate noise of 30% on the repeat mode and 24% on the random mode if the peak-to-peak voltages are concerned for both modes.

3.3 Frequency Dependence

The frequency dependence of the upper and lower peaks of the substrate noise voltage, together with its suppression ratio, $(V_{ppNoiseOFF} - V_{ppNoiseON})/V_{ppNoiseOFF}$, on the repeat mode are shown in Fig. 8(a) and on the random mode in Fig. 8(b). 17% to 34% of the substrate noise is suppressed from 100 MHz to 600 MHz operation range on the repeat mode, and 15% to 31% of the noise is suppressed on the random mode, by our feedforward active substrate noise cancelling circuit. The noise suppression ratio on the random mode does not degrade over 600 MHz operation since the dominant noise component becomes half of the operating frequency because of its random mode operation.

4. Discussion

4.1 Current Injection

The amplitude of the injected current for the noise cancelling is controlled by the noise canceller supply voltage

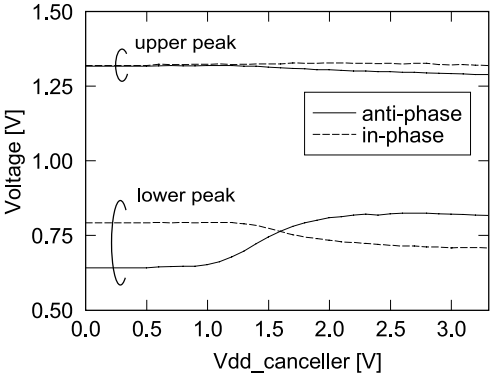

Fig. 9 Noise canceller supply voltage dependence of the substrate noise amplitude on the repeat mode at 500 MHz operation.

$Vdd\_canceller$, and $Vdd\_canceller$ dependence of the substrate noise is shown in Fig. 9. The graph shows the upper and lower peak voltage change at 500 MHz operation on the repeat mode. It is shown that the substrate noise starts to be reduced around 1.0 V as the cancelling signal increases until being saturated around 2.5 V at the anti-phase case. It is because the noise injection amplifier starts to operate over 1.0 V, and its gain is saturated around 2.5 V because the transconductance g_m of MP1 and MN1 saturates. The re-

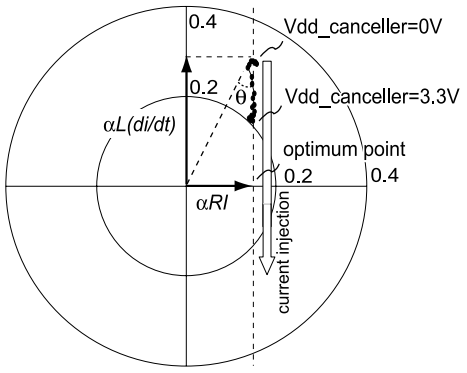

Fig. 10 Noise canceller supply voltage dependence of the substrate noise phasor, for *Vdd_canceller* sweeping from 0 V to 3.3 V by 0.1 V step, on the repeat mode at 500 MHz operation with the anti-phase current injection.

sults meet the HSPICE simulation results on which the amplifier starts to operate 1.05 V and the gain saturates around 2.55 V.

The phase and amplitude of the substrate noise is plotted in a phasor diagram as shown in Fig. 10. The phase is relative to $CLK/2$, and the radius corresponds to the substrate noise amplitude. The trace of the phasor with *Vdd_canceller* sweeping from 0 V to 3.3 V by 0.1 V step shows that more current injection by using bigger transistor width for MP1 and MN1 of the canceller amplifier suppresses more substrate noise until the optimum point which will achieve 56% noise reduction. Further current injection increases the substrate noise.

The amplitude and the phase of the original substrate noise is decided by the ground line impedance. We assumed that the ground line impedance is pure inductive, however, the real impedance has resistance component. So the substrate noise has the resistive component as well as the inductive component, and the resistive component remains since our cancelling technique is based on di/dt. If there is no resistive component, the phase of the substrate noise and di/dt match (i.e. θ=0), and it is possible that the substrate noise can be completely cancelled out.

Another type of injection circuit, whose plus-minus terminals of the amplifier inputs are exchanged to realize "in"-phase current injection, has also been implemented as a reference. Other circuits are exactly the same and the chip photograph looks the same as Fig. 5. The in-phase current injection increases the substrate noise as shown in Fig. 9 dashed line. The result supports the model that the substrate noise reduction in the previous section is realized by our feedforward active cancelling scheme, not by other reasons. The cause of the substrate noise difference between the anti-phase and the in-phase at *Vdd_canceller*=0 in Fig. 9 is considered as the process variation. Since the test chip for the anti-phase injection experiment and the test chip for the in-phase injection experiment are different, the offsets and gains of the noise probers become different.

4.2 Gain and Frequency Response

The DC gain and the cut-off frequency of the prober shown in Fig. 3 are 14 and 350 MHz, respectively, according to HSPICE simulations. The cut-off frequency looks so small, however, the gain of the prober at 1 GHz is 3 and it is enough to probe the substrate noise reduction ratio of the active cancel ON and OFF, especially for repeat mode experiment shown in Fig. 8(a).

In order to cancel the substrate noise, the gain of the canceller shown in Fig. 2 should be flat and the phase should be zero for the di/dt noise frequency component. According to HSPICE simulations, the cut-off frequency of the canceller is 3.3 GHz which is high enough for our test case.

However, the current injection (gain) is too small in our test case because our estimation was not accurate enough. In order to obtain the optimum point described in Fig. 10, the following methods are possible. For example, 1) the mutual inductor and canceller parameters are designed based on an accurate substrate noise estimation. 2) the canceller is designed to be large enough which enable too much current injection and dynamically control the canceller supply voltage or the canceller transistor sizes by a feedback with lower loop bandwidth based on the probed substrate noise amplitude.

4.3 di/dt Detection

We detect the di/dt of the power line, not the di/dt of the ground line, because the di/dt detector causes voltage bounce due to the parasitic impedance $R_1 + j\omega L_1$ shown in Fig. 2 [6]. The voltage bounce may cause additional substrate noise and our di/dt-based substrate noise cancelling effect may be disturbed if the di/dt detector is used for the ground line. Other than the metallized ground line, the ground node of the internal circuit has some paths to the external ground through the substrate. However, the di/dt from the power supply and the di/dt to the external ground are the same amount, hence the di/dt of the power supply is proportional to the substrate noise as long as inductance is dominant among the ground line impedance.

The parasitic impedance of the di/dt detector causes the power supply noise for the internal circuit. Since this is a feasibility experiment, we employ a conservative design on the mutual inductor structure. However, the noise voltage can be reduced with smaller resistance R_1 and inductance L_1 on the power supply line by using a thicker metal, multi-layer (ML2 and ML3 together, for example), wider and straight power supply line with a adjacent spiral inductor [6].

5. Conclusion

A feedforward active substrate noise cancelling based on di/dt of power supply has been demonstrated. When di/dt noise is dominant on the ground bounce, the substrate noise

is also proportional to di/dt since the digital ground line and the substrate are tied with low impedance. By injecting the minus di/dt-proportional current into the substrate using a power supply di/dt detector and the following amplifier, the substrate noise can be cancelled out. Our experimental results show that this cancelling technique suppresses 30% of the substrate noise on our 500 MHz operating test circuit, and 17% to 34% substrate noise reduction is achieved from 100 MHz to 600 MHz frequency range. The phasor diagram analysis shows that the optimum canceller design will enhance the noise suppression ratio up to 56%.

Acknowledgement

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References

[1] M. Takamiya, M. Mizuno, and K. Nakamura, "An on-chip 100 GHz-sampling rate 8-channel sampling oscilloscope with embedded sampling clock generator," IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers, pp.182–183, Feb. 2002.

[2] K. Makie-Fukuda, S. Maeda, T. Tsukada, and T. Matsuura, "Substrate noise reduction using active guard band filters in mixed-signal integrated circuits," IEICE Trans. Fundamentals, vol.E80-A, no.2, pp.313–320, Feb. 1997.

[3] T. Tsukada, Y. Hashimoto, K. Sakata, H. Okada, and K. Ishibashi, "An on-chip active decoupling circuit to suppress crosstalk in deep sub-micron CMOS mixed-signal SoCs," IEEE Int. Solid-State Circuit Conf. Dig. Tech Papers, pp.160–161, Feb. 2004.

[4] T. Nakura, M. Ikeda, and K. Asada, "Feedforward active substrate noise cancelling technique using power supply di/dt detector," JSAP/IEEE Symposium on VLSI Circuits, pp.284–297, June 2005.

[5] T. Nakura, M. Ikeda, and K. Asada, "Power supply di/dt measurement using on-chip di/dt detector circuit," IEEE/JSAP Symposium on VLSI Circuits, pp.106–109, June 2004.

[6] T. Nakura, M. Ikeda, and K. Asada, "On-chip di/dt detector circuit," IEICE Trans. Electron., vol.E88-C, no.5, pp.782–787, May 2005.

[7] "FastHenry USER'S GUIDE," [Online] Available: http://rleweb.mit.edu/vlsi/codes.htm

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