Autonomous di/dt Noise Control Scheme for Margin Aware Operation

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Abstract:

This paper demonstrates the first trial of an autonomous and margin aware di/dt noise control scheme. A di/dt on the power line is detected by a mutual inductor, the induced voltage is multiplied by Gilbert multiplier and the following low pass filter outputs a DC voltage in proportion to the di/dt noise. The DC voltage is compared with reference voltages, and the modes of the internal circuit is controlled depending on the comparators output. By using this scheme, the di/dt noise power can be autonomously controlled to fall within a defined range set by the reference voltages.
We use two operation modes here: all-active and half-active modes. Our experimental results show that the internal circuit oscillates between the all-active and the half-active modes, also show that the all/half ratio and the oscillation frequency changes depending on the reference voltages. It proves that our autonomous di/dt noise control scheme works as being designed.

1. Introduction

As the process technology advances, the number of transistors on an LSI chip has been increasing and their high speed operations generate more power line noise while the low supply voltage reduces the noise margin. Thus, the power line noise becomes a serious issue for the reliability of the LSI operations. The ground line noise also presents on the substrate[1] because the ground line and the substrate are tied with very low impedance, and hence the power line noise becomes a serious concern for substrate noise on analog-digital mixed signal LSIs as well. The noise on a power line is caused by di/dt noise and resistive voltage drops due to the parasitic impedance of the power line. As a chip operating frequency becomes higher, the di/dt noise becomes dominant. An EMI noise is also caused by the di/dt.
It is difficult to predict the amount of the di/dt noise by a circuit simulation because it requires a huge database of the parasitic impedance, the switching activity and the switching timing, along with very long simulation time. In addition, many recent LSIs have several operating modes. Moreover, a process variation often makes the prediction different from the actual di/dt noise[2].
This paper proposes an autonomous and margin aware di/dt noise control scheme. We have proposed an on-chip di/dt detector[3], and the di/dt detector can be used for the di/dt noise control scheme here since the detector is realized on-chip and outputs the di/dt value in real time. The first trial, as the authors knowledge, of the autonomous and margin aware di/dt noise control scheme is demonstrated here using 0.15μm 5-ML SOI-CMOS technology.

2. Circuit Design

2.1 Basic Concept

The block diagram of the autonomous di/dt noise control scheme is shown in Fig.1. The operation of the internal circuit causes the di/dt of the power line. The mutual inductor induces the di/dt proportional voltage between the terminals of the secondary inductor, the induced voltage is squared and the di/dt noise power waveform is obtained. And the following low pass filter outputs the DC voltage in proportion to the di/dt noise power. Then the comparators compare the DC voltage with reference voltages V_{refN}, and the operation mode controller controls the mode of the internal circuit in accordance with the comparator outputs. For example, the modes of the internal circuit include the variations of the clock frequency, effective power supply voltage, threshold voltage, number of the pipeline stage, number of parallel threading and so on. These mode changes result in different di/dt of the internal circuit and hence the di/dt noise of the internal circuit can be controlled.
Another advantage of this method is that the allowed di/dt level can be decided by the reference voltages of the comparators. Thus it is expected that a decided noise margin is autonomously realized by setting the proper reference voltages.

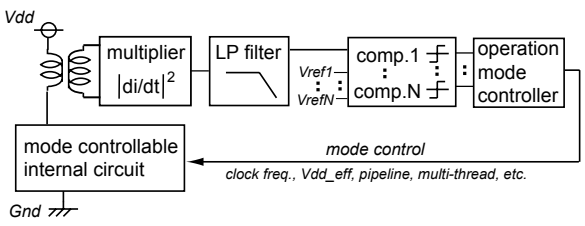

Figure 1: Block diagram of the autonomous di/dt noise control scheme.

2.2 Internal Circuit as Noise Source

Figure 2 shows our internal circuit as a noise generator. The circuit contains VCO so that we can easily sweep the clock frequency by changing the DC control voltage ($Vctrl$). The frequency divider generates 101010... signal for the input to the shift resister. The following dividers generates $CLK/4$, $CLK/8$ signals by which the DFF outputs and some inverter chains are disconnected when the divided clock outputs are "Low", and hence the current waveform becomes different in accordance with the divided clock signals. $allORhalf$ signal controls the activation ratio of the circuit. The $CLK/32$ output is used as a trigger for a oscilloscope, and the $CLK/2$ output is used to check if the circuit works fine.
Note that the internal circuit has two modes: the all-active and half-active modes.

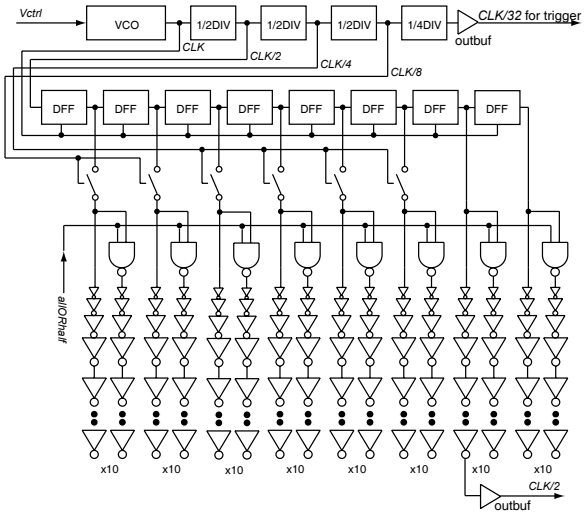

Figure 2: Internal circuit.

2.3 di/dt Detector

The di/dt detector here is a mutual inductor which induces the di/dt proportional voltage between the terminals. The mutual inductors here consists of a power supply line and an underlying spiral inductor. The power supply line L_1 is composed of the top metal layer ML5 with 1 turn, 20μm width. The spiral inductor L_2 has 20 turns with 2μm width and 2μm spacing using ML3. The outside diameter of the both inductors are 150μm $\times$ 150μm, as shown in Fig.3.
The resistors R_b are used to keep the DC bias voltage as half-Vdd for the following input. The resistor is formed using gate-poly without silicide and the resistance is 10kΩ which is big enough to be considered open for AC signal.

2.4 di/dt Multiplier and Low Pass Filter

A Gilbert multiplier[4] is used for obtaining the square of the di/dt signal, which converts the di/dt proportional voltage into the di/dt noise power waveform. The following low pass filter is composed of a resistor and a capacitor. The schematic is shown in Fig.4.

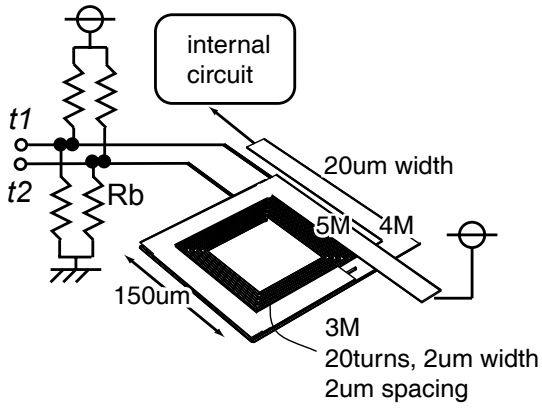

Figure 3: Mutual inductor structure.

The analog output current of the multiplier is proportional to $(V_{in1} - V_{in2}) \times (V_{in3} - V_{in4})$. Here, $in1$ and $in3$ in Fig.4 are connected to $t1$ in Fig.3, and $in2$, $in4$, $t2$ are connected so that the output signal is proportional to the di/dt noise power.
The resistor of the low pass filter is formed using gate-poly without silicide and the resistance is about 100kΩ, the capacitor is formed using MIM capacitor and the capacitance is about 2.5pF.

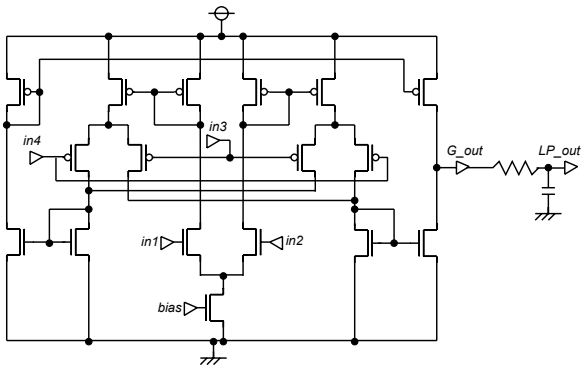

Figure 4: Gilbert multiplier and low pass filter.

2.5 Comparators and Operation Mode Controller

The comparator compares the di/dt noise power voltage with the reference voltage, and outputs "H" if the di/dt noise power voltage is higher than the reference voltage. We use two comparators and the reference voltages are V_{refL} and V_{refH}.
The schematic of the operation mode controller is shown in Fig.5. When the di/dt noise power is lower than V_{refL} (inL=inH="L"), the operation mode controller outputs "H(all)" to the $allORhalf$ node so that all the internal circuit is turned on. When the di/dt noise power is higher than the threshold V_{refH} (inL=inH="H"), the operation mode controller outputs "L(half)" to the $allORhalf$ node so that the half of the internal circuit is turned off and the di/dt is reduced. When the di/dt noise power is between V_{refH} and V_{refL}, the operation mode controller outputs the signal so as to keep the previous operation mode.

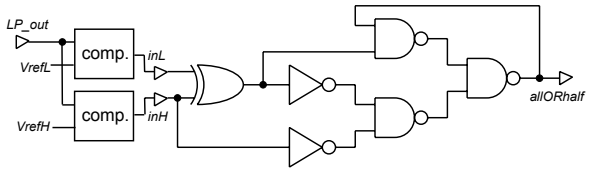

Figure 5: Schematic of the operation mode controller.

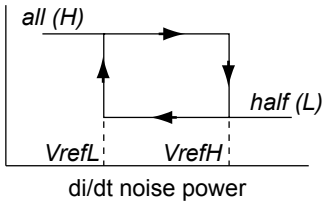

Figure 6: Operation of the hysteresis comparator.

Thus, the comparators and the operation mode controller consist of a hysteresis comparator, as shown in Fig.6.

3. Measurement

3.1 Setups

The chip is designed and fabricated using 0.15μm 5-ML SOI-CMOS technology, and the chip area is about 3.2mm$\times$1.8mm, as shown in Fig.7.
The chip is mounted on a Cu board as shown in Fig.8. All the inputs are DC and supplied through lead lines to the "islands" on the board. The voltage of the islands are stabilized by several chip capacitors. 50Ω transmission lines are directly connected to the high-speed output pins including $CLK/2$, $CLK/32$. The $allORhalf$ signal is probed by a high impedance (1MΩ) probe.

3.2 Frequency Dependence of di/dt Noise Power

When the same reference voltage is applied to V_{refH} and V_{refL}, and sweeping the voltage, the $allORhalf$ signal changes when the reference voltage crosses the low pass filter output voltage which reflects the di/dt noise power. (Actually $allORhalf$ oscillates at a range of the reference voltage, which will be described in the next section, the center voltage is used here as the low pass filter output voltage, and hence the di/dt noise power.)

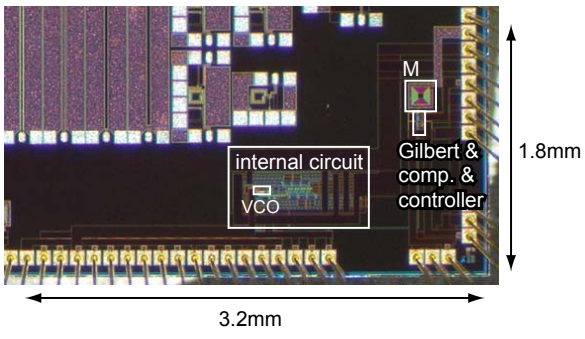

Figure 7: Chip photograph.

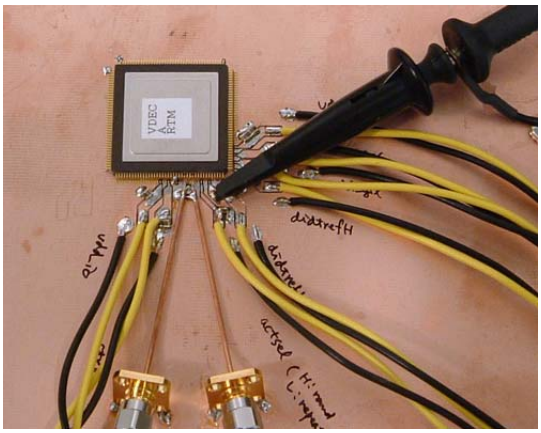

Figure 8: Measurement Setup.

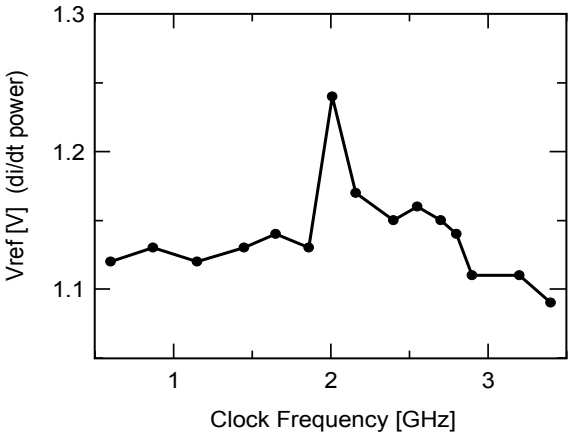

Figure 9: Clock frequency dependence of the di/dt noise power.

The clock frequency dependence of the di/dt noise power under 1.5V power supply is shown in Fig.9. It shows that the di/dt noise power has a peak at around 2.0GHz, which reflects the package and the bonding wire characteristics.

4. Discussions

4.1 Waveforms of Oscillation

As being described, the internal circuit has two modes: the all-active and half-active modes. If the di/dt noise power of the all-active is higher than V_{refH} and the di/dt noise power of the half-active is lower than V_{refL}, the internal circuit oscillates between the two modes. The H/L ratio depends on the average of the reference voltages $(V_{refL} + V_{refH})/2$, and the higher reference voltages lead higher H ratio. The oscillation frequency depends on the reference voltage difference $V_{refH} - V_{refL}$ (and the low pass filter time constant), and the bigger reference voltage difference leads longer oscillation period.
The oscillation waveforms of $allORhalf$ signal between the all-active(H) and the half-active(L) modes are shown in Fig.10. The clock frequency is set to 2.0GHz in this measurement where the maximum di/dt is obtained as shown in Fig.9.

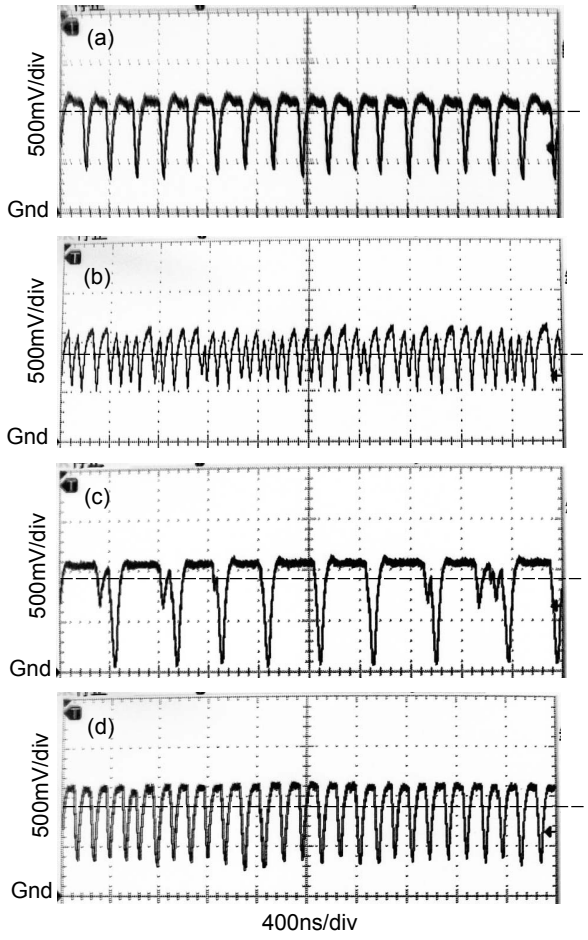

Figure 10: Measured waveforms of $allORhalf$ signal at 2.0GHz clock frequency. The applied reference voltages, the measured results are summarized in Table 1.

	V_{ref} avrg.[V]	ΔV_{ref}[V]	Out[V]	period[ns]
(a)	1.275	0.01	1.0	222
(b)	1.270	0.00	0.9	91
(c)	1.270	0.02	0.9	444
(d)	1.265	0.01	0.9	148
	1.250	1.28	L	–
	1.260	1.29	H	–

Table 1: Reference voltage dependence of the oscillation period when the clock frequency is 2.0GHz.

The applied reference voltages, the measured H/L ratio and the oscillation period of (a), (b), (c) and (d) cases of Fig.10 are summarized in Table 1. Since the output driver of the $allORhalf$ signal is so small that the average output voltage of the waveforms is used here as the indication of the H/L ratio.
For the H/L ratio, though the difference of case (b) and (c) is not clear because the ΔV_{ref} is not the same, the difference between (a) and (d) is clear and reasonable. For the oscillation period, it is clear that the oscillation period becomes longer as ΔV_{ref} becomes larger.

No oscillation occurs and stays "L" when $V_{refL} \leq 1.25$V and stays "H" when $V_{refH} \geq 1.29$V because the all-active has the di/dt noise power of 1.29-δ[V] and half-active has the di/dt noise power of 1.25+δ[V] where $0 < \delta < 0.01$V.

5. Conclusions

An autonomous and margin aware di/dt noise control scheme has been demonstrated. A di/dt on the power line is detected by a mutual inductor, the induced voltage is squared by the Gilbert multiplier and the following low pass filter outputs the DC voltage in proportion to the di/dt noise power. The DC voltage is compared with reference voltages, and the mode of the internal circuit is controlled depending on the comparators output.
Though we used only two operation modes in this study. it can be easily extended to multiple operation modes. Our experimental results show that the mode of the internal circuit oscillates among the different operation modes so that the average di/dt noise power falls within a region determined by the reference voltages. It proves that our autonomous di/dt noise control scheme works as being designed.
This is the first demonstration, as the authors knowledge, of an autonomous and margin aware di/dt noise control scheme.

Acknowledgments

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