On-chip di/dt Detector Circuit for Power Supply Line

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Abstract — This paper describes an on-chip di/dt detector circuit for power supply line. The di/dt detector consists of a spiral inductor under the power supply line and a noise-tolerant amplifier. The former induces di/dt proportional voltage by means of the mutual inductive coupling, and the latter amplifies the induced voltage linearly. Simulation results show that the detector can measure the di/dt with the accuracy of 1.52×10^7A/s. The current waveform can be obtained by integrating the di/dt, and the result shows 0.72mA accuracy at the average current of 50mA.

Introduction

As the process technology advances, the transistor count in a LSI chip has been increasing, the operating frequency has been getting higher, and the supply voltage has been getting lower. Thus, the power supply noise is getting a critical issue from the signal integrity point of view.

Recently, a di/dt noise is becoming a dominant source of the power supply noise along with an IR drop. An EMI noise also becomes a serious problem for high speed operating LSIs. In order to estimate these noises, current measurement techniques, especially high frequency di/dt measurement techniques, are urgent to be developed in order to keep the reliability of the LSI functions.

Many techniques have been proposed to measure the power supply voltage fluctuation[1][2]. On the other hand, only few techniques have been developed for the power supply current measurement. One technique uses a resistor connected in series to a power supply line on a PCB board and measure the voltage difference of the both terminal using electron-beam probing[3]. This technique needs numerical calculation to obtain the current and di/dt waveforms. Another technique picks up the magnetic field and measure the spectrum[4]. It is unable to reproduce the original current nor di/dt waveforms from the spectrum because the phase information is lost.

This paper proposes an on-chip di/dt measurement technique. This technique can be applicable to control the LSI system operations dynamically according to the observed di/dt, such as operating frequency and power supply voltage, because the detector is realized on-chip and outputs the di/dt value itself.

di/dt Detector Structure

A. Basic Concept

Figure 1 shows the block diagram of the di/dt detector circuit. A power supply current for the internal circuit goes through the power supply line inductance L_1. A pickup inductance L_2 coupled to L_1 with a coupling coefficient K induces a di/dt proportional voltage. A noise-tolerant amplifier amplifies the induced voltage and outputs to a 50Ω transmission line that enables a high frequency measurement.

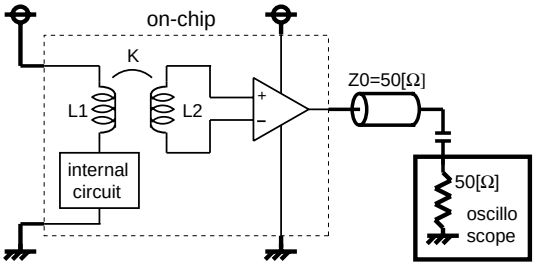

Fig. 1. Block diagram of the di/dt detector circuit. The bold lines represent outside devices.

B. Mutual Inductor

The inductance L_1 should be small since it is in series connection to the power supply line. The small inductance requires a high coupling coefficient K and a bigger L_2 in order to generate the enough induced voltage on the terminal of L_2.

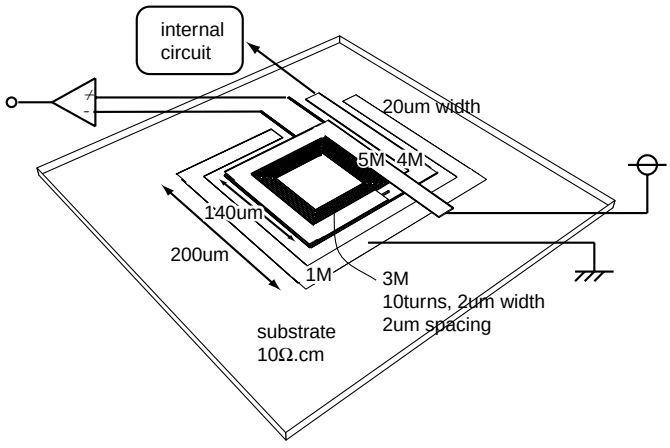

Fig. 2. Mutual inductor structure.

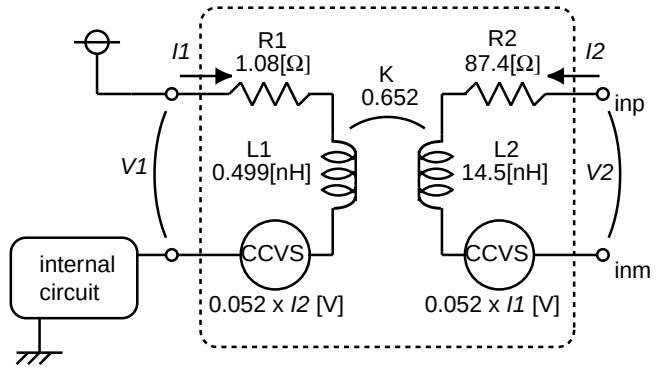

Fig. 3. Equivalent circuit.

We assumed a 0.18μm 5 metal layer CMOS process with the target frequency of 2GHz. Figure 2 shows our mutual inductor structure. We decided the outline of the inductors as $200 \times 200\mu m^2$, which is about two times as big as a bonding pad size.

The spiral inductor of the third layer metal(M3) is placed under the one turn power supply line of the top layer metal(M5) in order to derive a high coupling coefficient. The spiral inductor has 10 turns with 2μm width and 2μm spacing. The total length of the spiral inductor is 3.922mm which is 0.051λ, where λ is the wavelength of 2GHz signal. It is short enough to be considered as a lump element instead of a distributed element. We do not have to concern the bigger parasitic resistance on the spiral inductor, as will be described later.

The equivalent circuit of this mutual inductor structure is extracted by FastHenry[5] as shown in Fig.3.

Mutual inductance M is expressed as

$$M = K\sqrt{L_1 L_2} \tag{1}$$

whose value becomes 1.76nH. The output voltage V_2 from the mutual inductor is

$$V_2 = M\frac{dI_1}{dt} + R_2 I_2 + L_2\frac{dI_2}{dt}. \tag{2}$$

This equation can be interpreted as the electromotive force $M\frac{dI_1}{dt}$, and the output impedance R_2 and L_2. The spiral inductor L_2 is connected to the amplifier, whose inputs *inp* and *inm* are terminated by NMOS gates with 10kΩ pull-up and pull-down resistors, which are enough high impedance compared with the output impedance R_2, L_2 so that the output impedance can be negligible and the eqn(2) can be approximated to $V_2 = M\frac{dI_1}{dt}$.

C. Amplifier, Output Buffer and Measurement Structure

Since the output di/dt value is a high speed analog signal, the following points are the key issues for the amplifier design.

- High frequency amplification with high linearity
- High frequency signal output to the 50Ω transmission lines
- Noise immunity

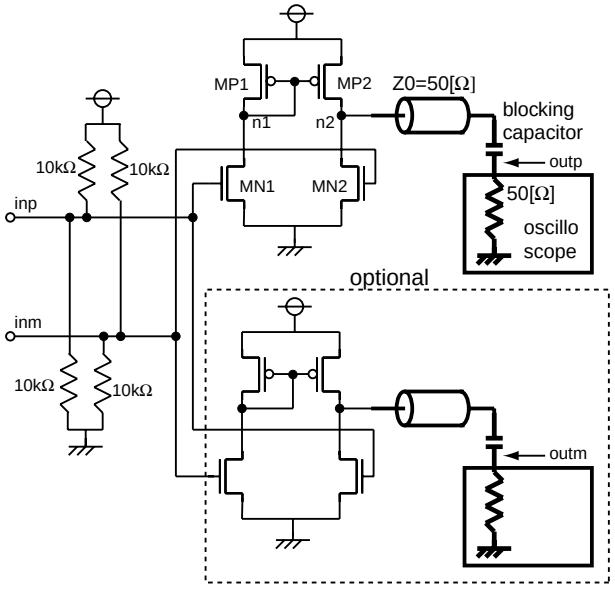

Fig. 4. Amplifier/Output buffer, and measurement setup.

Note that the average of di/dt value is zero, otherwise the current value would be infinity.

Figure 4 shows our structure. The output pins are connected to the 50Ω transmission lines. We employed current mirror type amplifiers without current source, and the bias voltage of the input is half-vdd which realizes the maximum gain. The half-vdd is generated by the pull-up and pull-down 10kΩ resistors. Blocking capacitors are inserted at the input ports of the oscilloscope to prevent from the bias point change of the node $n2$ due to the 50Ω termination resistor connected to GND.

We did not use feedback type amplifiers because they cannot respond to the high frequency signals. Moreover, the 50Ω load is too small to keep the linearity of the amplifier gain even if feedback amplifiers are employed. The open loop amplifiers cannot control the gain by additional components. The characteristics, however, can be predicted by a circuit simulation.

As for the noise immunity, the amplifier itself is vdd-noise insensitive. Assuming that the power supply has ΔV_n noise. The noise on both *inp* and *inm* nodes are the same as $\Delta V_n/2$, which is not amplified since the amplifier amplifies the voltage difference between *inp* and *inm* nodes. Also, the *inp*, *inm* change has small sensitivity to the output. The PMOS and NMOS size are designed so as the internal node *n1* and *n2* is biased as $vdd/2$, where the maximum gain is realized. The NMOS input voltage and the node $n1$ moves to $(vdd + \Delta V_n)/2$ by the ΔV_n noise. The Gate-Source voltage change of both MP2 and MN2 is the same as $\Delta V_n/2$. Thus, the current change of both MP2 and MN2 is the same, and no current flows to the termination resistor, which means no noise occurred at the output terminal.

The amplifier does not have a symmetric structure. We can, however, eliminate the asymmetrical characteristics and increase the linear operation range and the gain by using two amplifiers with plus-minus exchanged inputs and measure the difference of the output. Unexpected common-mode noises can also be eliminated with this structure. The second amplifier

is optional and the one-amplifier structure is enough if the one-amplifier gain, the linear range and the noise tolerance meet the specification of your di/dt measurement.

Figure 5 shows an DC simulation result of the amplifier. The amplifier has the linearity of ±300mV/200mV input range with the gain of 1.273/0.637 for two/one-amplifier structure, respectively. The cut-off frequency is over 10GHz according to an AC simulation, which is high enough for our purpose.

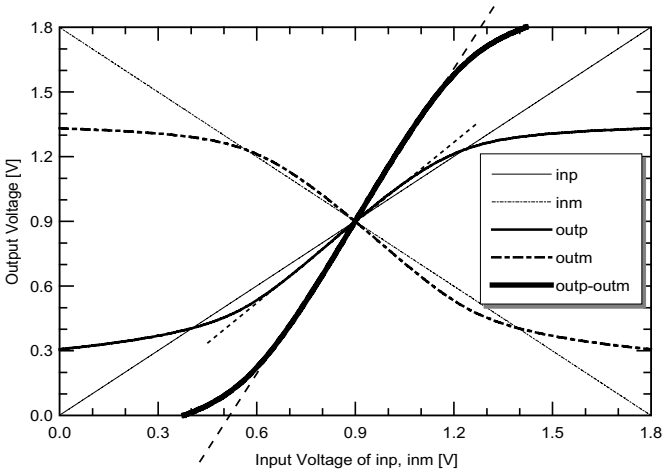

Fig. 5. DC characteristic of the amplifier.

D. di/dt sensitivity

Assuming that the gain of the amplifier is G,

$$V_{outpm} \equiv V_{outp} - V_{outm} = G(V_{inp} - V_{inm}) \tag{3}$$

and neglecting the parasitics of the spiral inductor from eqn(2),

$$V_2 = V_{inp} - V_{inm} = K\sqrt{L_1 L_2}\frac{dI_1}{dt} \tag{4}$$

these equations lead

$$\frac{dI_1}{dt} = \frac{1}{GK\sqrt{L_1 L_2}} V_{outpm} \tag{5}$$

$$V_{outpm} = GK\sqrt{L_1 L_2}\frac{dI_1}{dt} \equiv A_{didt2vout}\frac{dI_1}{dt} \tag{6}$$

According to the FastHenry extraction of the mutual inductance and HSPICE simulation of the amplifier gain, the value of L_1, L_2, K and G are 0.499×10^{-9}H, 14.5×10^{-9}H, 0.652 and 1.273/0.637, so the $A_{didt2vout}$ becomes $2.23 \times 10^{-9}/1.12 \times 10^{-9}\Omega$·s in our di/dt detector with the two/one-amplifier, respectively.

The input range limitation $\pm V_{in\_lim}$ of the amplifier decided by the linearity restricts the detectable di/dt range as

$$\frac{di}{dt}_{lim} = \pm\frac{1}{K\sqrt{L_1 L_2}} V_{in\_lim} \tag{7}$$

and the resolution of the output voltage V_{out_res} restricts the detectable di/dt resolution as

$$\frac{di}{dt}^{res} = \frac{1}{GK\sqrt{L_1 L_2}} V_{out\_res}. \tag{8}$$

We can control the detectable range and the resolution by adjusting the mutual inductor and the amplifier design.

Simulation Results

A. Test Circuit

Figure 6 shows our internal circuit as a noise generator. The DFF chain shifts 101010... signal. The SEL circuit can select the operating mode, a repeat mode and a random mode. On the repeat mode, the SEL circuit always outputs "High" signal, all the inverter chains have input changes at every clock cycle, and the circuit consumes the same current waveform at every clock cycle. On the random mode, the SEL circuit pass the CLK/4, CLK/8 signals, the DFF output are blocked for some inverter chain, and the current waveform is different in accordance with the divided clock signals.

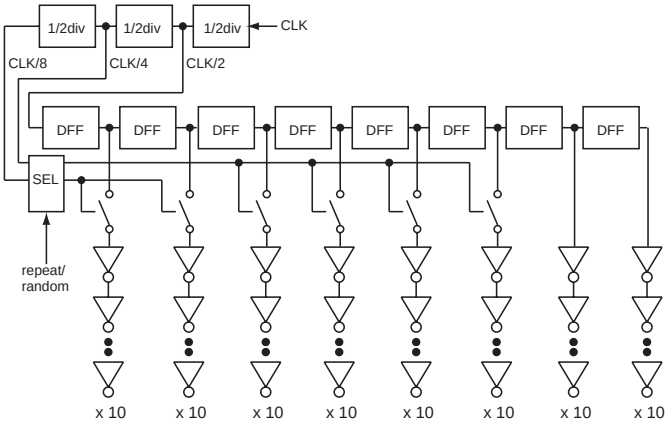

Fig. 6. Internal circuit. Select the repeat/random mode by SEL.

The whole test circuit was designed by connecting the mutual inductor, the two-amplifier and the test circuit shown in Fig.3, 4 and 6. Also, 1nH inductors representing a package parasitic inductance are attached to all the output pins, as shown in Fig.7.

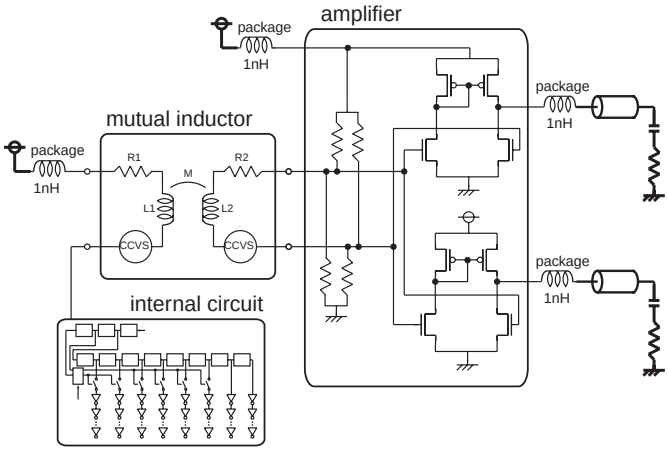

Fig. 7. Whole test circuit.

B. Waveforms

Simulation waveforms are shown in Fig.8(a) for the repeat case, and (b) for the random case. The output voltage of V_{outpm} and the numerically-differentiated di/dt multiplied by $A_{didt2vout}$ are shown at the same time.

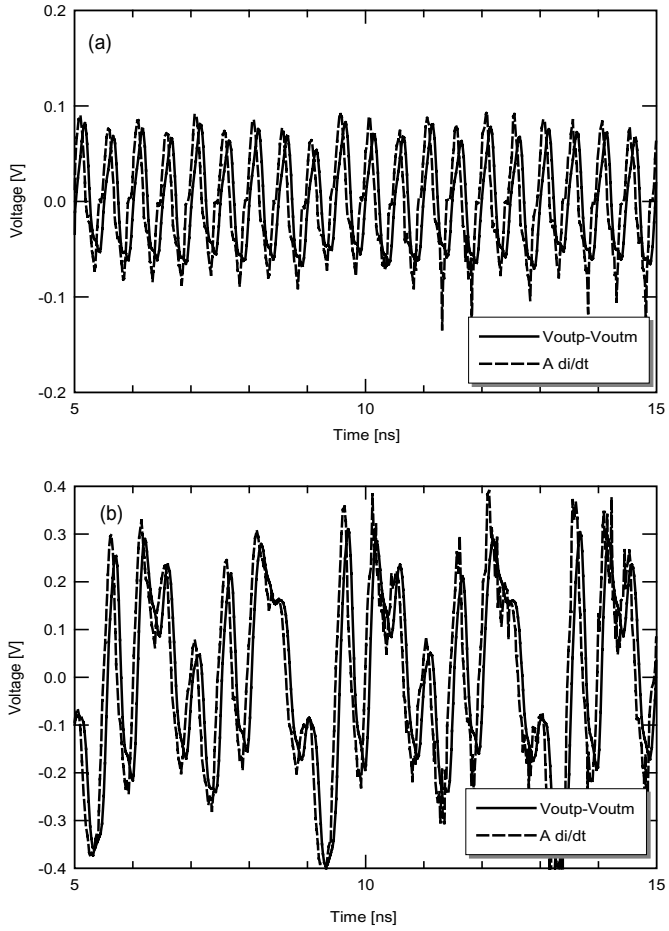

Fig. 8. Simulated waveforms of the V_{outpm} and the numerically-differentiated di/dt multiplied by $A_{didt2vout}$ for (a) repeat case σ=6.8mV(3.05×10^6A/s), and for (b) random case σ=34mV (1.52×10^7A/s).

Integrating the eqn(5) with respect to time,

$$I_1 = \int \frac{1}{GK\sqrt{L_1L_2}} V_{outpm}dt \equiv \frac{1}{A_{didt2vout}} \int V_{outpm}dt. \quad (9)$$

The simulated I_1 and numerically-integrated $\int V_{outpm}dt$ divided by $A_{didt2dout}$ on the random case are shown in Fig.9.

We can see that both di/dt, V_{outpm} and I_1, $\int V_{outpm}dt$ match well, as predicted from eqn(6) and eqn(9). The spike noise on the dashed lines in Fig.8 comes from the numerical canceling. The time shift between the solid lines and the dashed lines come from the delay of the amplifier.

The standard deviation σ between the solid lines and the dashed lines after shifting the x-axis so as to cancel the delay in Fig.8(a), (b) and Fig.9 are, 6.8mV(3.05×10^6A/s), 34mV(1.52×10^7A/s) and 0.72mA, respectively.

These results show that di/dt can be measured by probing the output voltage, and the time-integration of the output voltage waveform produces the current waveform as well.

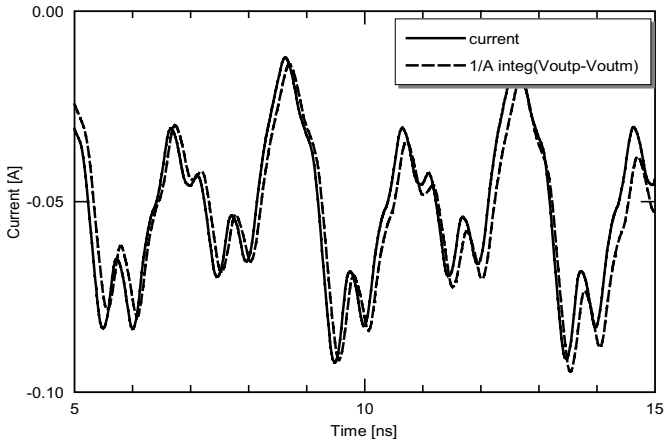

Fig. 9. Simulated waveforms of the I_1 and the numerically-integrated $\int V_{outpm}dt$ divided by $A_{didt2vout}$. σ=0.72mA.

Conclusion

An on-chip di/dt detector for power supply line has been demonstrated. The di/dt detector consists of a spiral inductor under the power supply line and a noise-tolerant amplifier. The former induces di/dt proportional voltage by means of the mutual inductive coupling, and the latter amplifies the induced voltage linearly. Simulation results show that the detector can measure the di/dt with the accuracy of 1.52×10^7A/s. The current waveform can be obtained by integrating the di/dt, and the result shows 0.72mA accuracy at the average current of 50mA on our test circuit. In addition, we can adjust the detectable di/dt range and the resolution by changing the spiral inductor and the amplifier design.

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