A Study on
Power Line Noise Reduction
in Large Scale Integration

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Chapter 1

Introduction

As the process technology has been advanced to the deep submicron, both the number of transistors integrated per area and the chip size have been increased continuously. In addition, higher operating frequency and higher interconnect overall capacitances increase the power supply current of an LSI.

At the same time, reduction of the power supply voltage, which is driven by several factors such as reduction of power dissipation, reduced transistor channel length and reliability of gate dielectrics, reduces the noise margin of the supply voltage. Table 1.1 shows the future prediction of power supply voltage and power consumption according to ITRS road map[1], and saying that 0.5V power supply and 251W power consumption which means the power supply current as high as over 500A are expected to be achieved by 2013. The large current can cause large noise for LSIs and turns up the signal integrity issues.

The basic approach for designing a robust LSI is to design a low impedance power supply. The power supply voltage bounce caused by the impedance and the power supply current leads unpredictable timing violations or even logical failures. Not only average supply voltage drop but also peak voltage drop should be suppressed.

The main source of the power supply noise was IR drop caused by the resistance of

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<tbody>
<tr>
<td>Vdd [V]</td>
<td>1.0</td>
<td>1.0</td>
<td>0.9</td>
<td>0.9</td>
<td>0.7</td>
<td>0.6</td>
<td>0.5</td>
<td>0.4</td>
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<tr>
<td>Power (High-performance [W])</td>
<td>150</td>
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<td>170</td>
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<td>104</td>
<td>120</td>
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<td>158</td>
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<tr>
<td>Power (Battery [W])</td>
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<td>3.2</td>
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<td>3.5</td>
<td>3.5</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
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the power line and the power supply current. Recently, $\frac{di}{dt}$ noise caused by the power line inductance and the power supply current change is becoming dominant as the chip operating frequency is getting higher. Therefore, not only lower impedance of the power line, but also reducing the supply current change ($\frac{di}{dt}$) are effective to suppress the power supply noise.

There have been many researches for power supply voltage bounce or power line impedance extractions while only few attentions have been paid for power supply current nor $\frac{di}{dt}$. The $\frac{di}{dt}$ plays an important role for the power supply noise and also electromagnetic interference (EMI) noise on a LSI with its faster clock frequency. Stricter electromagnetic compatibility (EMC) regulations have been enforced recently[2]. Although electromagnetic radiation occurs mainly from cables, connectors, printed circuit board (PCB) wires, LSI packages and so on, the ultimate noise source is gate switching in LSIs. The dominant EMI noise is a radiation from the power lines of the LSI. The power supply current flows to the power layers on the PCB and the power cables, and the electromagnetic radiation occurs from these off-chip conductors. Note that EMI radiation is caused by $\frac{di}{dt}$, not by voltage perturbation. Thus $\frac{di}{dt}$ is important for EMI analysis and EMI control as well as for power supply voltage fluctuation analysis.

The growing demand for multimedia applications requires large-scale integration of accurate analog circuits with many high-speed digital circuit gates. In these analog-digital mixed signal integrated circuits, substrate noise is becoming critical to restrict the chip performance. Although power supply lines for digital blocks and analog blocks are separated each other to prevent the noise coupling, both the analog and digital circuits are fabricated on the same chip with the common substrate. Thus the analog blocks are suffered from the crosstalk of the digital switching noise through the substrate.

Guard band is the most common way to reduce the substrate noise. This technique puts substrate contacts around the analog block and the contacts are connected to an external ground so that the noise from the digital blocks is absorbed into the external ground instead of transferred to the analog block. However, the parasitic inductance of the guard line degrades the noise absorption effects for high frequency noise. Another method is feedback active guard band filtering, in which the anti-phase noise signal is actively supplied to the guard band so that the original substrate noise is cancelled out. In this technique, an amplifier is used to sense the original substrate noise and generate the anti-phase noise signal. This technique, however, does not work well for high frequency noise neither, because the feedback system restricts the response bandwidth.

Substrates are tied to power supply lines, and hence the substrate noise is closely related to the power supply noise in which $\frac{di}{dt}$ noise is dominant.
Therefore a $di/dt$ reduction and a $di/dt$ measurement techniques are urgent to be developed in order to improve the signal integrity for high speed LSIs. Also the $di/dt$ measurement technique can be applicable for substrate noise reduction since substrate noise is closely related to $di/dt$.

This paper focuses on power line noise reduction caused by $di/dt$.

Chapter 2 proposes to use stubs instead of decoupling capacitors to reduce power supply noise. A comparison between stubs and decoupling capacitors, and conditions where stubs are more effective than the decoupling capacitors are theoretically given.

Chapter 3 shows experimental results of the power supply noise reduction of stubs. Although the noise reduction effect was not clearly observed with an on-chip stub, clear noise reduction effects and their frequency dependence were observed with on-board stubs.

An on-chip $di/dt$ detector for power supply line is described in Chap.4. $di/dt$ and current waveforms obtained from the $di/dt$ detector output and a series resistor voltage difference were compared, and had good agreement.

In Chap.5, a feedforward active substrate noise cancelling technique is introduced. The $di/dt$ detector circuit described in Chap.4 is applied to generate an anti-phase signal against the substrate noise, and the anti-phase signal cancels out the substrate noise if it is injected into the substrate.

Finally in Chap.6, the studies on power line noise reduction in LSIs are summarized and discussed for the conclusion of this paper.
Chapter 2

Comparison of Stubs and Decoupling Capacitors for Noise Reduction

Abstract

This chapter compares stubs and decoupling capacitors for power supply noise reduction. A quarter-length stub attached to the power supply line of an LSI chip works as a band-eliminate filter, and suppresses the power supply bounce of the designed frequency. The conditions where the stub is more effective than the same-area decoupling capacitor are clarified. It is theoretically shown that the stub will work more efficiently and on-chip integration will be possible on high frequency operation LSIs.
2.1 Introduction

Power supply noise is caused by the power line impedance and the supply current. Along with IR drop, \( di/dt \) noise caused by the power line inductance and the current change \((di/dt)\) is becoming critical as the chip operating frequency advances. Power supply voltage drops cause unpredictable timing violations or even logical failures. For example, 10% voltage drop leads about 15% delay increase when \( V_{th} \) equals 0.3\( V_{dd} \) because gate delays are proportional to \( 1/(V_{dd} - V_{th}) \) [3]. Also the supply voltage bounce changes the logic threshold and the output voltage level of the gates, resulting a logical failure if the transceiver gate output voltage and the receiver gate logic threshold move toward different directions at the same time. Therefore, not only average supply voltages drop but also peak voltage drops should be suppressed. At the same time, electromagnetic compatibility (EMC) regulations have been enforced recently[2], where Electromagnetic Interference (EMI) noise radiated by \( di/dt \) is dominant.

In order to suppress the power supply noise and \( di/dt \), some methods such as a semi-synchronous architecture[4], using a complicated PCB board design[5] have been proposed. These methods, however, make circuit designs complex and difficult. The most common way to suppress power supply noise and \( di/dt \) is to use decoupling capacitors between the power and the ground lines[6]. However, chip capacitors do not work well in high frequency because of their parasitic inductance of the terminals, and on-chip capacitors require more die area.

A quarter-length stub attached to the power supply line of an LSI chip works as a band-eliminate filter, and suppresses the power supply bounce of the designed frequency as shown in Fig.2.1. Stubs are widely used for impedance matching technique of wireline communications, where the loss of the transmission lines are ignored. Lossy transmission lines have been studied but only for signal wires[7].

![Figure 2.1: Stub \( di/dt \) reduction.](image-url)
This chapter compares stubs and decoupling capacitors for power supply noise and $\frac{di}{dt}$ reduction.

In Sect.2.2, the basic stub theorem is explained. Section 2.3 presents analytical models of stubs and decoupling capacitors, and compares the power supply noise reduction effects. Discussions are given in Sect.2.5, and Sect.2.6 summarizes this chapter. Section 2.7 is an appendix to describe equations associated with stubs.

### 2.2 Stub Theorem

The notations in Table 2.1 will be used in this section.

#### 2.2.1 $\lambda/4$ Stub Basics

A quarter length stub works as a band-eliminate filter. This section derives the equations for the stub.

As the operation frequency becomes higher and the wavelength of voltage and current get comparable with the wire length, the wire should be considered as a transmission line instead of lumped RC elements. The characteristic impedance $Z_0$, the propagation constant $\gamma$ of the transmission line are

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (2.1)$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (2.2)$$

$$\equiv j\beta_c = \alpha + j\beta_r \quad (2.3)$$

where $R, L, G, C$ are the resistance, inductance, admittance representing the dielectric loss, capacitance of the wire, per unit length respectively. $G = 0$ is assumed in this chapter.

The forward- and backward- going waves are expressed as $V_f e^{-\gamma z}, V_b e^{\gamma z}$. This expression can be transformed using phase constant $\beta_c$ and attenuation constant $\alpha$,

$$V_f e^{-\gamma z} \equiv V_f e^{-\alpha z} e^{-j\beta_z} = V_f e^{-(\alpha + j\beta_c) z} = V_f e^{-j\beta_r - j\alpha z}. \quad (2.4)$$

This equation leads that

$$\alpha = \text{real}(\gamma), \quad \beta_c = \text{imag}(\gamma) \quad (2.5)$$

and the complex phase constant $\beta_c$ is defined as

$$\beta_c = \beta_r - j\alpha. \quad (2.6)$$
Table 2.1: Notations for Stub Theorem.

<table>
<thead>
<tr>
<th>Notation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>$R$</td>
<td>resistance per unit length of the stub</td>
</tr>
<tr>
<td>$L$</td>
<td>inductance per unit length of the stub</td>
</tr>
<tr>
<td>$G$</td>
<td>admittance per unit length of the stub</td>
</tr>
<tr>
<td>$C$</td>
<td>capacitance per unit length of the stub</td>
</tr>
<tr>
<td>$Z_0$</td>
<td>characteristic impedance</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>propagation constant</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>attenuation constant</td>
</tr>
<tr>
<td>$\beta_r$</td>
<td>phase constant without loss</td>
</tr>
<tr>
<td>$\beta_c$</td>
<td>phase constant with loss</td>
</tr>
<tr>
<td>$\Gamma_s$</td>
<td>reflection coefficient at the near end</td>
</tr>
<tr>
<td>$\Gamma_f$</td>
<td>reflection coefficient at the far end</td>
</tr>
<tr>
<td>$Z_{stub}$</td>
<td>stub input impedance</td>
</tr>
<tr>
<td>$\lambda_0$</td>
<td>voltage, current wavelength in the stub</td>
</tr>
<tr>
<td>$\varepsilon_0$</td>
<td>dielectric constant in the vacuum</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>relative dielectric constant</td>
</tr>
<tr>
<td>$c$</td>
<td>velocity of light in the vacuum</td>
</tr>
<tr>
<td>$\eta$</td>
<td>round trip attenuation factor</td>
</tr>
<tr>
<td>$Z_{lEquiv}$</td>
<td>equivalent termination impedance</td>
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</tbody>
</table>

With using the complex phase constant, the forward- and backward- going wave are written as $V_r e^{-j\beta_c z}$ and $V_r e^{j\beta_c z}$, which are familiar expressions to us. Note that we can consider the loss and phase in the different parameters ($\alpha, \beta_r$), or in one parameter which is the complex propagation constant $\beta_c$.

The reflection coefficient $\Gamma$ of the characteristic impedance $Z_0$ and the termination impedance $Z_l$ is

$$\Gamma = \frac{Z_l - Z_0}{Z_l + Z_0}. \quad (2.7)$$

The input impedance of the transmission line with its characteristic impedance $Z_0$, length $l$ and termination impedance at the far end $Z_l$ is

$$Z_{stub} = Z_0 \frac{Z_l \cos \beta_c l + jZ_0 \sin \beta_c l}{Z_0 \cos \beta_c l + jZ_l \sin \beta_c l}. \quad (2.8)$$

When open termination ($Z_l = \infty$),

$$Z_{stub} = Z_0 \frac{\cos \beta_c l}{j \sin \beta_c l}. \quad (2.9)$$
If the transmission line has no loss \((R = G = 0)\) and its length is quarter of the signal wavelength \((\beta_c l = \pi/2)\), the input impedance of the stub becomes zero \((Z_{stub} = 0)\), which is equivalent with an infinite capacitance. When this stub is attached to the power line, the voltage fluctuation is suppressed.

The dominant frequency of the switching current is the clock frequency \(f_0\). Thus, the stub length adjusted for the clock frequency becomes

\[
l = \frac{\pi/2}{\beta_{r0}} = \frac{\lambda_0}{4} = \frac{c/\sqrt{\epsilon_r}}{4f_0}
\]

where \(\lambda_0\), \(c\) and \(\epsilon_r\) are the signal wavelength in the transmission line, the speed of light in vacuum and the relative dielectric constant. Once the stub length is decided for the frequency \(f_0\), the stub absorbs the noise of the frequency \((2n - 1)f_0\) as well, as known from eqn(2.9) since

\[
\cos(\beta_cl) \approx \cos[(2n-1)\beta_{r0}l] = \cos\left(\frac{(2n-1)\pi}{2}\right) = 0.
\]

Another stub, whose length is \(l/2\), can be attached at the same time for the second dominant frequency \(2f_0\) and \((2n - 1) \cdot 2f_0\).

### 2.2.2 Equivalent Termination Approximation

If the wire is ideal in which the resistance is zero,

\[
Z_{0\text{ideal}} = \sqrt{\frac{L}{C}}
\]

\[
\alpha_{\text{ideal}} = 0
\]

\[
\beta_{\text{ideal}} = \omega \sqrt{LC} = \beta_r.
\]

Since the impedance of the power line is small, the resistance of the stub is not negligible. The round trip attenuation factor \(\eta\) caused by the propagation loss in the lossy line is

\[
\eta = e^{-\alpha_{2l}}.
\]

The propagation loss is the only loss when lossy line with an open termination, while the reflection is the only loss when lossless (ideal) line with a finite termination impedance. Here, we propose a concept of equivalent termination impedance \(Z_{l\text{Equiv}}\) which induces a loss at the reflection \(\Gamma_{l\text{Equiv}}\) with the ideal line, as the same amount of the round trip propagation loss \(\eta\) with the lossy line. In other words, we can consider the stub as a no-resistance ideal wire with \(Z_{l\text{Equiv}}\) termination, instead of a resistive wire with open termination, as shown in Fig.2.2.

\[
\eta = \Gamma_{l\text{Equiv}} \equiv \frac{Z_{l\text{Equiv}} - Z_{0\text{ideal}}}{Z_{l\text{Equiv}} + Z_{0\text{ideal}}},
\]
From this equation, the equivalent impedance value becomes

\[ Z_{I\text{Equiv}} = Z_{0\text{Ideal}} \frac{1 + \eta}{1 - \eta} = \sqrt{\frac{L}{C}} \frac{1 + \eta}{1 - \eta} \]

(2.17)

then from eqn(2.8), the input impedance of the quarter length stub \((\beta l = \pi/2)\) becomes

\[ Z_{\text{stubEquiv}} = Z_{0\text{Ideal}} \frac{Z_{I\text{Equiv}} \cos(\frac{\pi}{4}) + jZ_{0\text{Ideal}} \sin(\frac{\pi}{4})}{Z_{0\text{Ideal}} \cos(\frac{\pi}{4}) + jZ_{I\text{Equiv}} \sin(\frac{\pi}{4})} \]

(2.18)

\[ = Z_{0\text{Ideal}} \frac{1 - \eta}{1 + \eta} = \sqrt{\frac{L}{C}} \frac{1 - \eta}{1 + \eta} \]

(2.19)

2.3 Analytical Models of Stubs and Decoupling Capacitors

The notations in Table 2.2 will be used in this section.

2.3.1 Stub and Capacitor Impedance

As shown in the previous section, the stub input impedance does not become zero even if the length is adjusted for \(\lambda/4\) because of the parasitic resistance of the wire. A wider stub reduces the resistance, however, a larger area is required and the same-area decoupling capacitor may have the same noise reduction effects. This section compares the stub and the capacitor input impedance with the same area \(A\). The thickness of the stub wire is \(t\), the
Table 2.2: Notations for Analytical Models.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$l$</td>
<td>stub length</td>
</tr>
<tr>
<td>$w$</td>
<td>stub width</td>
</tr>
<tr>
<td>$t$</td>
<td>stub, capacitor thickness</td>
</tr>
<tr>
<td>$d$</td>
<td>distance between the upper and the lower plates</td>
</tr>
<tr>
<td>$A$</td>
<td>stub, capacitor area</td>
</tr>
<tr>
<td>$\rho$</td>
<td>resistivity of the wire</td>
</tr>
<tr>
<td>$\delta$</td>
<td>skin depth</td>
</tr>
<tr>
<td>$C_{total}$</td>
<td>total capacitance of the plates</td>
</tr>
<tr>
<td>$Z_{0l}$</td>
<td>characteristic impedance at lower frequency</td>
</tr>
<tr>
<td>$Z_{0h}$</td>
<td>characteristic impedance at higher frequency</td>
</tr>
<tr>
<td>$Z_{stub}$</td>
<td>stub input impedance</td>
</tr>
<tr>
<td>$Z_{sl}$</td>
<td>stub input impedance at lower frequency</td>
</tr>
<tr>
<td>$Z_{sh}$</td>
<td>stub input impedance at higher frequency</td>
</tr>
<tr>
<td>$Z_{cap}$</td>
<td>capacitor input impedance</td>
</tr>
<tr>
<td>$f_R$</td>
<td>frequency at which skin effects appear</td>
</tr>
<tr>
<td>$f_C$</td>
<td>frequency at which $w = d$</td>
</tr>
<tr>
<td>$f_D$</td>
<td>frequency at which $\omega l = R$</td>
</tr>
<tr>
<td>$f_S$</td>
<td>frequency at which $Z_{sl} = Z_{sh}$</td>
</tr>
<tr>
<td>$f_B$</td>
<td>boundary frequency at which $Z_{stub} = Z_{cap}$</td>
</tr>
<tr>
<td>$\tau$</td>
<td>time constant from $Z_0$ to $Z_{stub}$</td>
</tr>
<tr>
<td>$\Gamma_s$</td>
<td>reflection coefficient at the stub near end</td>
</tr>
<tr>
<td>$\Gamma_l$</td>
<td>reflection coefficient at the stub far end</td>
</tr>
</tbody>
</table>

distance between the signal and the ground line is $d$, the length and the width are $l$ and $w$, the resistivity of the stub are $\rho$ and the relative dielectric constant is $\epsilon_r$, as shown in Fig.2.3. The relative permeability $\mu_r$ is assumed to be 1.

From $A = lw$ and eqn(2.10),

$$w = \frac{4Af}{\sqrt{\epsilon_r}c},$$

(2.20)
Figure 2.3: Stub and the same-area decoupling capacitor.

Figure 2.4: Current distribution in a wire with the skin effect. (a) $t \leq 2\delta$ or $w \leq 2\delta$, (b) $2\delta < w < t$, (c) $2\delta < t < w$. 
The resistance per unit length $R$ becomes

$$R = \begin{cases} \frac{\rho}{wt} \times 2 = \frac{\rho c}{2Af \sqrt{\varepsilon_r}} & (t \leq 2\delta \text{ or } w \leq 2\delta) \\ \frac{\rho}{2\delta t} \times 2 = \sqrt{\frac{\rho \pi f}{\varepsilon_r c^2 t^2}} & (2\delta < w < t) \\ \frac{\rho}{w2\delta} \times 2 = \sqrt{\frac{\rho \pi}{16A^2 \varepsilon_r \varepsilon_0 f}} & (2\delta < t < w) \end{cases}$$

(2.21)

where $\delta = \sqrt{\frac{2\rho}{(\omega \mu_0)}}$ is the skin depth, and approximated that the uniform current flows within the skin depth as shown in Fig.2.4 gray part, and no current flows at the center and the hatched part neither for simplicity. The ”×2” is because the signal and the ground resistors are merged, and eqn(2.20), $c = 1/ \sqrt{\mu_0 \varepsilon_0}$ are used. The conditions to become (a), (b) and (c) in Fig.2.4 will be described later.

The capacitance per unit length $C$ becomes

$$C = \begin{cases} \frac{\pi \varepsilon_r \varepsilon_0}{\log \frac{d}{w_2}} & (w < d \Rightarrow f < f_c) \\ \frac{\pi \varepsilon_r \varepsilon_0}{\log \frac{c d}{\sqrt{\varepsilon_r \varepsilon_0}}} & (w \leq d \Rightarrow f_c \leq f) \end{cases}$$

(2.22)

$$f_c = \frac{cd}{4A \sqrt{\varepsilon_r}}$$

(2.23)

using the parallel cylinder line capacitance model[8] for $w < d$ case and the parallel plate model for $d \leq w$ case. $f_c$ is the frequency at which $w = d$, and eqn(2.20) is used. Note that discontinuity happens at the transition from the parallel cylinder model to the parallel plate model. Since $c/ \sqrt{\varepsilon_r} = 1/ \sqrt{LC}$,

$$L = \begin{cases} \log \frac{c d}{2A \sqrt{\varepsilon_r}} & (w < d \Rightarrow f < f_c) \\ \frac{c^2 \pi \varepsilon_0}{4 \varepsilon_c c A f \sqrt{\varepsilon_r}} & (d \leq w \Rightarrow f_c \leq f) \end{cases}$$

(2.24)

The characteristic impedance becomes

$$Z_0 = \begin{cases} Z_{0lf} = \sqrt{\frac{R}{j \omega C}} & (\omega L < R \Rightarrow f < f_D) \\ Z_{0hf} = \sqrt{\frac{L}{C}} & (R \leq \omega L \Rightarrow f_D \leq f) \end{cases}$$

(2.25)

$$f_D = \frac{R}{2\pi L}$$

(2.26)

where $f_D$ is the frequency at which $\omega L = R$.

The stub input impedance becomes its characteristic impedance if the total wire resistance $R \times l$ is bigger, while the input impedance goes close to zero if the total wire
impedance is small enough, and approximated to $Rl/2$\cite{9}. Since the total wire resistance reduces as the frequency increases,

$$Z_{stub} \simeq \begin{cases} 
Z_{slf} = Z_{0lf} = \sqrt{\frac{R}{j\omega C}} & (f < f_S) \\
Z_{shf} = \frac{R}{2l} & (f_S \leq f)
\end{cases} \quad (2.27)$$

where $f_S$ is the frequency at which $|Z_{0lf}| = Rl/2$, and (2.21), (2.10) are used.

The input impedance of the same-area decoupling capacitor is

$$Z_{cap} = \frac{1}{j\omega C_{total}} = \frac{d}{j2\pi f\epsilon_r\epsilon_0 A} \quad (2.29)$$

where the resistance is ignored and the ideal parallel plate model is adopted here. The ratio of $|Z_{stub}|$ and $|Z_{cap}|$ is

$$\frac{|Z_{stub}|}{|Z_{cap}|} = \begin{cases} 
|Z_{slf}| & (f < f_S) \\
|Z_{shf}| & (f_S \leq f)
\end{cases} \quad (2.30)$$

Note that $|Z_{slf}| < |Z_{shf}|$ holds for $f < f_S$, so the relation of

$$\frac{|Z_{stub}|}{|Z_{cap}|} \leq \frac{|Z_{shf}|}{|Z_{cap}|} \quad (2.31)$$

holds for all frequency. Therefore we use $Z_{shf}$ as the stub impedance for the comparison with the capacitor, and it is a stub-pessimistic evaluation. The ratio becomes

$$\left| \frac{Z_{shf}}{Z_{cap}} \right| = \begin{cases} 
\frac{\pi c^2 \epsilon_0 \rho}{8tf} & (t < 2\delta \text{ or } w < 2\delta) \\
\frac{\pi^3 \epsilon_r \epsilon_0 \rho A^2 f}{16 t^2 d^2} & (2\delta < w < t) \\
\frac{\pi^3 c^2 \epsilon_0 \rho}{256 d^2 f} & (2\delta < t < w)
\end{cases} \quad (2.32)$$

using eqn(2.21), (2.27) and (2.29). Note that the ratio decreases as the frequency goes higher on the first and the third conditions of eqn(2.32) while the ratio increases on the second condition as shown in Fig.2.5(ii).

The boundary frequency $f_B$ at which $Z_{shf} = |Z_{cap}|$ is

$$f_B = \begin{cases} 
\frac{\pi c^2 \epsilon_0 \rho}{8td} & (t < 2\delta \text{ or } w < 2\delta) \\
\frac{\pi^3 \epsilon_r \epsilon_0 \rho t^2 A^2}{16 \delta^2 d^2} & (2\delta < w < t) \\
\frac{\pi^3 c^2 \epsilon_0 \rho}{256 \delta^2 d^2} & (2\delta < t < w)
\end{cases} \quad (2.33)$$

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Figure 2.5: Simplified graph of $|Z_{stub}/Z_{cap}|$. (i) when $t^3 \leq \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi}$, and (ii) when $t^3 > \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi}$.

Here, the relations for $t$, $w$ and $\delta$ are

(a) $t \leq 2\delta$ or $w \leq 2\delta$

$\Rightarrow \begin{cases} \frac{t^3}{A} \leq \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi} \quad \text{and} \quad f \leq f_{R1} \\
\frac{t^3}{A} > \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi} \quad \text{and} \quad f \leq f_{R2} \end{cases}$  \hspace{1cm} (2.34)

(b) $2\delta < w < t$

$\Rightarrow \begin{cases} \frac{t^3}{A} > \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi} \quad \text{and} \quad f_{R2} < f < f_{R0} \end{cases}$  \hspace{1cm} (2.35)

(c) $2\delta < t < w$

$\Rightarrow \begin{cases} \frac{t^3}{A} \leq \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi} \quad \text{and} \quad f_{R1} < f \\
\frac{t^3}{A} \geq \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi} \quad \text{and} \quad f_{R0} \leq f \end{cases}$  \hspace{1cm} (2.36)

\begin{align*}
f_{R0} &= \frac{ct}{4A\sqrt{\varepsilon_r}}, \quad f_{R1} = \frac{4\rho c^2 \varepsilon_0}{\pi t^2}, \quad f_{R2} = \sqrt{\frac{\rho c^4 \varepsilon_0}{4\pi A^2 \varepsilon_r}} \tag{2.37}
\end{align*}

where $f_{R0}$, $f_{R1}$ and $f_{R2}$ is the frequency at which $w = t$, $2\delta = t$ and $2\delta = w$, respectively. Note that $w < t$ at $f < f_{R0}$, and $w > t$ at $f > f_{R0}$. Also note that the case (b) $2\delta < w < t$ does not occur when $\frac{t^3}{A} \leq \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi}$, as shown in Fig.2.5(i).

The relations which $f_B$ falls within the conditions of eqn(2.34), where the case (i)-(β), (ii)-(β) or (ii)-(γ) in Fig.2.5, are

\begin{align*}
\begin{cases} \frac{t^3}{A} \leq \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi} \quad \text{and} \quad t \leq \frac{32d}{\pi^2} \\
\frac{t^3}{A} > \frac{16\rho\sqrt{\varepsilon_r\varepsilon_0}c}{\pi} \quad \text{and} \quad t^3 \geq \frac{\pi^2\varepsilon_r\varepsilon_0\rho^2 A^2}{128d^3} \end{cases} \tag{2.38}
\end{align*}

and the relations which $f_B$ falls within the conditions of eqn(2.35), where the case (ii)-(β)
in Fig.2.5, are
\[
\frac{t^3}{A} > \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad \frac{\pi^3 c^2 \varepsilon_\varepsilon_0 \rho^2 A^2}{128d^3} < t^3 < \left( \frac{\pi^3 c \sqrt{\varepsilon_\varepsilon_0} \rho A}{64d^2} \right)^3
\]  
(2.39)

and the relations which \( f_B \) falls within the conditions of eqn(2.36), where the case (i)-(\( \alpha \)), (ii)-(\( \alpha \)) or (ii)-(\( \beta \)) in Fig.2.5, are
\[
\begin{align*}
\frac{t^3}{A} &\leq \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad t > \frac{32d}{\pi^2} \\
\frac{t^3}{A} &> \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad t \leq \frac{\pi^3 c \sqrt{\varepsilon_\varepsilon_0} \rho A}{64d^2}
\end{align*}
\]  
(2.40)

using eqn(2.34), (2.35), (2.36) with \( f = f_B \) of eqn(2.33). Note that \( \frac{\pi^3 c^2 \varepsilon_\varepsilon_0 \rho^2 A^2}{128d^3} < \left( \frac{\pi^3 c \sqrt{\varepsilon_\varepsilon_0} \rho A}{64d^2} \right)^3 \) is always true when \( \frac{t^3}{A} > \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \). Here, the conditions of eqn(2.39) is included in the conditions of both eqn(2.38) and (2.40). Thus, \( |Z_{shf}/Z_{cap}| = 1 \) occurs at three frequencies if eqn(2.39) holds, as shown in Fig.2.5(ii)-(\( \beta \)). In this case, the boundary frequency above which the stub input impedance is lower than the capacitor input impedance is the frequency of \( f_{BC} \) in Fig.2.5(ii)-(\( \beta \)). Therefore, the boundary frequency for the condition of eqn(2.39) is merged into the condition of eqn(2.40), in other words, the case (ii)-(\( \beta \)) is merged into the case (ii)-(\( \alpha \)), and results to
\[
f_B = \frac{\pi^3 c^2 \varepsilon_\varepsilon_0 \rho}{8td} \quad \text{if} \quad \frac{t^3}{A} \leq \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad t \leq \frac{32d}{\pi^2} \]  
(2.41)

\[
\begin{align*}
\frac{t^3}{A} &\leq \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad t \leq \frac{32d}{\pi^2} \\
\frac{t^3}{A} &> \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad t > \frac{\pi^3 c \sqrt{\varepsilon_\varepsilon_0} \rho A}{64d^2}
\end{align*}
\]  
(2.42)

\[
f_B = \frac{\pi^3 c^2 \varepsilon_\varepsilon_0 \rho}{256d^2} \quad \text{if} \quad \frac{t^3}{A} \geq \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad t > \frac{32d}{\pi^2} \]  
(2.43)

\[
\begin{align*}
\frac{t^3}{A} &\leq \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad t > \frac{32d}{\pi^2} \\
\frac{t^3}{A} &> \frac{16\rho \sqrt{\varepsilon_\varepsilon_0}c}{\pi} \quad \text{and} \quad t \leq \frac{\pi^3 c \sqrt{\varepsilon_\varepsilon_0} \rho A}{64d^2}
\end{align*}
\]  
(2.44)

The stub input impedance becomes smaller than the decoupling capacitor input impedance above the boundary frequency \( f_B \), and if the LSI operating frequency is higher than the boundary frequency, the stub suppresses the noise more efficiently than the decoupling capacitor with the same required area.

### 2.3.2 Numerical Analysis

In order to validate the analysis above, the numerical calculation was carried out as follows. For the given area \( A \), the wire thickness \( t \), the distance \( d \), the resistivity \( \rho \) and the relative...
The frequency dependence of the characteristic impedance, the stub and the capacitor input impedance, and the stub resistance per unit length are shown in Fig. 2.6, where \( d = 5 \mu m, t = 1 \mu m, A = 1 \text{mm}^2, \epsilon_r = 3.9, \rho = 1.673 \times 10^{-8} \Omega \cdot \text{m} \) are used here as an example.

Dielectric constant \( \epsilon_r \), the stub length is decided for a given frequency \( f \) from eqn(2.10). The stub width \( w \) is decided by eqn(2.20). Then the inductance \( L \) and the capacitance \( C \) per unit length of this structure are extracted using Raphael\[10\] 2D field solver. The resistance \( R \) per unit length is extracted using FastHenry\[11\] 3D field solver in which the resistance and the skin effects are taken into consideration. Then we estimate the stub input impedance by eqn(2.1)-(2.9), and the capacitor input impedance is calculated by eqn(2.29).

The frequency dependence of the characteristic impedance, the stub and the capacitor input impedance, and the resistance per unit length are shown in Fig.2.6, where \( d = 5 \mu m, t = 1 \mu m, A = 1 \text{mm}^2, \epsilon_r = 3.9 \) in SiO\(_2\) with Cu wire \( \rho = 1.673 \times 10^{-8} \Omega \cdot \text{m} \) are used here as an example. Figure 2.7 shows the frequency dependence of the stub and the capacitor input impedance ratio with different parameter values, The markers are numerical simulation results and the lines are the analytical results, showing that the analytical models agree well with the numerical simulation results. Note that the step at \( f_C \) in Fig.2.6 comes from the discontinuity of the capacitor model expressed by eqn(2.22). The dashed lines are using \( Z_{stub} = Z_{shf} \) even for \( f < f_S \), showing that eqn(2.31) holds. The slope of the stub input impedance is \( S_{stub} = -2 \) and \(-1.5 \) for \( f_S \leq f \leq f_R \) and \( f_R < f \), the slope of the capacitor impedance is \( S_{cap} = -1 \), as being derived as eqn(2.10), (2.21), (2.27) and (2.29). Then in
Figure 2.7: Input impedance ratio of the stub and the decoupling capacitor with changing a parameter. The standard parameters are $d = 5\mu m$, $t = 1\mu m$, $A=1\text{mm}^2$, $\epsilon_r=3.9$, $\rho = 1.673 \times 10^{-8} \Omega \cdot \text{m}$.

Figure 2.8: Frequency dependence of the input impedance of the stub designed for 2.5GHz and the capacitor.
Fig. 2.7, $S_r$, the slope of the $|Z_{stub}/Z_{cap}|$, is −1 and −0.5 for $f \leq f_R$ and $f_R < f$, respectively. These results indicate that the stub structure becomes more efficient over the capacitor as the frequency goes higher.

The stub with $d = 5\mu m$, $t = 1\mu m$, $A = 1\text{mm}^2$, $\epsilon_r = 3.9$, $\rho = 1.673 \times 10^{-8}\Omega \cdot \text{m}$ is adjusted for a 2.5GHz operation LSI as our theoretical test case whose stub structure becomes $w = 66\mu m$, $l = 15.181\text{mm}$, $L = 83.9\text{nH/m}$, $C = 517\text{pF/m}$, $R = 532\Omega/\text{m}$ and $C_{total} = 6.91\text{pF}$. The frequency dependence of the input impedance of the stub and the capacitor with this structure are shown in Fig. 2.8. This graph also shows that the stub input impedance is smaller than the capacitor impedance around the designed frequency.

In order to confirm that the stub suppresses the power supply noise better than the decoupling capacitor when $|Z_{stub}/Z_{cap}| < 1$, circuit simulation using this stub will be carried out in the next section.

2.4 Circuit Simulation

2.4.1 Internal Circuit

A PRBS (Pseudo Random Bit Stream) $2^7 - 1$ generation circuit with an inverter chain at each output of the DFF, as shown in Fig. 2.9, is used as our test internal circuit. The circuit represents a common synchronous circuit. The PRBS pattern and the inverter chains represent a random switching of an LSI and combination logics, respectively. The length of the inverter chains distributes from 2 to 12, which represents a path length distribution between DFFs.

We tested three types of power line structures as the reference: nothing attached, the decoupling capacitor and the stub. The inductance of the lead frame and the bonding wire is assumed to be $1\text{nH}$, as shown in Fig. 2.9. The stub values are the same as the example in the previous section.

2.4.2 Simulation Results

Figure 2.10(a) shows HSPICE simulation waveforms of the virtualVdd node in Fig. 2.9 for each of the three power line structures, and (b) shows the corresponding spectrum, at 1.8V 2.5GHz operation. The standard deviation $\sigma$ from 1.8V ideal supply voltage is used as a measure of the noise amplitude.

$$\sigma = \sqrt{\frac{1}{T} \int_{t_0}^{T+t_0} (V_{\text{virtualVdd}} - V_{\text{idealVdd}})^2 dt}$$

(2.45)
Figure 2.9: Internal circuit. A PRBS generator and inverter chains with three kinds of power line structures.
Figure 2.10: (a) Simulated waveforms of the virtual\textit{Vdd} node. (b) Corresponding spectrum.
where $T$ is $2^7 - 1 = 127$ clock cycle period. The $\sigma$ values are 0.127, 0.097, 0.080 for the nothing, capacitor, stub case respectively. This means that the stub suppressed 37%, 18% of the noise compared with the nothing, capacitor case. Also, the stub suppressed 46%, 24% of the 2.5GHz noise component compared with the nothing, capacitor case, respectively, as shown in Fig.2.10(b).

The above power supply noise reduction ratios are not equal to the input impedance ratio (57%) of the stub and the decoupling capacitor since the power supply noise depends not only on the stub or the capacitor input impedance but also the parasitic impedance of the package and the parasitic capacitor of the internal circuit, and so on.

### 2.4.3 Voltage Swing at the End Terminal

The stub suppresses the noise because it stores and provides the energy of the designed frequency so that the less AC current component goes through the lead frame and the bonding wire inductance. The energy is stored by swinging the signal voltage in the stub, and the far end terminal has the maximum voltage amplitude. The ratio of the AC voltage amplitudes at the near end and the far end is

$$\frac{V_{far}}{V_{near}} \approx -j \frac{1 + \eta}{1 - \eta}$$

at the steady state as being derived as eqn(2.135), where $\eta$ is the round trip attenuation factor $e^{-\alpha \cdot 2l}$. The ratio is 3.38 on our stub. When the stub is used in an LSI, the attention should be paid so as not to exceed the break down voltage of the insulator between the metal layers, since the voltage at the end terminal becomes higher than the supply voltage. Since the stub input impedance is insensitive with the distance $d$ between the signal and the gnd, the thickness of the insulator could be increased if needed.

Figure 2.11(a) shows the simulated waveforms of the near end and the far end of the stub, and (b) shows the corresponding spectrum. These graphs show that the stub far end voltage has 3.14 and 3.08 times larger voltage swing than the near end around 2.5GHz and 7.5GHz, respectively, which means that the stub stores the energy around the frequencies, not around 5GHz. The result agrees with the frequency dependence of the stub shown in Fig.2.8, and the theoretical value from eqn(2.46) of 3.38.
Figure 2.11: (a) Simulation waveforms of the near end (virtualVdd) and the far end of the stub. (b) The corresponding spectrum.
2.5 Discussion

2.5.1 Simulation Technique

The stub can be modeled as a $RLC$ ladder as shown in Fig.2.2(a) for SPICE simulations. However, the number of the ladder step have to be big in order to suppress the $LC$ resonant ringing which does not occur in reality. Also, the inductors make simulation convergence difficult and take longer simulation time. By the equivalent termination approximation using an ideal transmission line element with the equivalent termination impedance as described in Subsec.2.2.2, the simulation time decreased 13% in our test case. A W element can be used if HSPICE[12] is used for the simulation. Figure 2.12 shows the simulated waveforms of the $virtualVdd$ node using a 100 stage LCR ladder, an ideal transmission line (T element) with the equivalent termination impedance and a W element as the stub, respectively. The HSPICE simulation gives very similar waveforms in these three cases, showing that the equivalent termination approximation is precise enough.

![Figure 2.12: HSPICE simulation waveforms of the virtualVdd node using 100 stage LCR ladder, T element with the equivalent termination impedance, and W element as the stub.](image-url)
2.5.2 Time Constant

The input impedance of the stub is $Z_0$ at the initial state, and $Z_{stub}$ at the steady state. It needs time constant $\tau$ to change the input impedance from $Z_0$ to $Z_{stub}$. Since the the near end impedance $Z_s$ is connected in parallel to the stub for the noise source current $I_0$, the current of the forward-going wave $I_f$ in the stub at the initial condition is,

$$I_f(t = 0) = \frac{Z_s}{Z_s + Z_0} I_0. \quad (2.47)$$

Since the forward-going wave is increased at the reflections which occur every half clock period $1/(2f)$, the current $I_f$ at a time $t$ becomes

$$I_f = \frac{Z_s}{Z_s + Z_0} \left(1 + -\eta \Gamma_s + \cdots + (-\eta \Gamma_s)^{2ft}\right) I_0 \quad (2.48)$$

$$= \frac{Z_s}{Z_s + Z_0} \cdot \frac{1 + \eta \Gamma_s(-\eta \Gamma_s)^{2ft}}{1 + \eta \Gamma_s}. \quad (2.49)$$

where $\Gamma_s = (Z_s - Z_0)/(Z_s + Z_0)$ is the reflection coefficient at the near end, $\eta$ is the round trip attenuation factor $e^{-\alpha \cdot 2l}$, the round trip phase rotation is $\pi$ and $e^{-j\pi} = -1$. Here,

$$(-\eta \Gamma_s)^{2ft} = e^{2ft \log |\eta \Gamma_s|} e^{j2ft \phi} \quad (2.50)$$

using $a^{bx} = e^{bx \log a}$ and $\log z = \log|z| + j \arg z$. It shows that the time constant is expressed as

$$\tau = \frac{1}{-2f \log |\eta \Gamma_s|}. \quad (2.51)$$

The current of the backward-going wave has the same time constant, so that the voltage and the impedance of the stub have the same time constant as well. Note that $|\eta \Gamma_s| \leq 1$, $\log |\eta \Gamma_s| \leq 0$ and $\tau$ is positive. The time constant is 453ps which is less than two clock cycle in our test case.

2.5.3 Frequency Components

If all the gates would switch at the same timing in every clock cycle, the current would contain only $nf_0$ components. However, practical circuits switch randomly at each clock cycle and cause non-$nf_0$ components. These components are suppressed more robustly by the capacitor. In addition, the capacitor may suppress the higher order $nf_0$ components better than the stub, as shown in Fig.2.8 other than around 2.5GHz, and even 7.5GHz case.

The stub reduces the power supply noise better than the capacitor since $f_0$ component is dominant in this example. However, if the non-$nf_0$ components or the higher order frequencies increase, the decoupling capacitor is better than the stub.
2.5.4 Higher Frequency Case

Since the stub length \( l \propto f^{-1} \), the stub width \( w \propto f \), and the skin depth \( \delta < f^{-0.5} \), the stub input impedance becomes \( Z_{stub} = RL/2 \propto f^{-2} \) or \( f^{-1.5} \) before and after \( f_R \) at which skin effect starts to appear, while the capacitor input impedance becomes \( Z_{cap} \propto f^{-1} \). The ratio becomes \( |Z_{stub}/Z_{cap}| \propto f^{-1} \) or \( f^{-0.5} \), as expressed by eqn(2.32). Therefore the stub has more advantage over the capacitor as the operating frequency goes higher, as shown in Fig.2.6 and Fig.2.7.

The stub input impedance \( Z_{stub} \) in our example is 4.00Ω while \( |Z_{cap}| = 9.22 \) and \( |Z_{stub}/Z_{cap}| = 0.43 \) at 2.5GHz with \( A=1\text{mm}^2 \). If the frequency becomes 10 times higher, 25GHz for example, with the same \( d, t, A, \epsilon_r \) and \( \rho \), the impedances become \( Z_{stub} = 0.089 \), \( |Z_{cap}| = 0.922 \), \( |Z_{stub}/Z_{cap}| = 0.097 \) and show that the stub advantage ratio increases \( 0.43/0.097=4.43 \) times which is in between \( 10^{0.5} \sim 10^1 \). When the distance \( d \) is reduced to \( 1\mu m \), the impedances become \( Z_{stub} = 0.091 \), \( Z_{cap} = 0.184 \) and the stub still keeps the advantage over the capacitor at this frequency.

The capacitance per unit area may be increased by using lateral capacitors together with the vertical capacitors, such as a comb capacitor[13], depending on \( d, t \) and the line-to-line space. However, the frequency dependence of the capacitor input impedance \( Z_{cap} \propto f^{-1} \) is the same and the advantage of the stub at high frequency still holds.

2.5.5 Stub Usage

The stub is designed on-chip in this paper. On-package or on-PCB board stubs can also suppress the noise. A smaller resistance stub using a thicker metal layer of the package or of the PCB board can realize more effective noise suppression. However, the parasitic inductance of the lead frame and the bonding wire could be the noise source when the on-package or on-PCB board stubs are used.

Some devices, especially mobile ones, require dynamic operating frequency control, and the stub length should be adjusted in accordance with the operating frequency in such cases. A variable inductor or capacitor on the stub end termination instead of the open termination can virtually control the stub length by changing the phase rotation at the reflection.

2.6 Summary

Stubs and decoupling capacitors have been compared for power supply noise reduction. A quarter-length stub attached to the power supply line of an LSI chip works as a band-
eliminate filter, and suppresses the power supply bounce of the designed frequency. The boundary frequency above which the stub is more effective than the same-area decoupling capacitor is clarified.

The circuit simulation results show that the stub reduces 37% and 18% of the power supply noise compared with the nothing attached case, and the decoupling capacitor case, respectively, in our 1.8V 2.5GHz test circuit with \( d = 5\mu m, t = 1\mu m, A=1mm^2, \varepsilon_r=3.9, \rho = 1.673 \times 10^{-8}\Omega\cdot m \) case.

Theoretical study shows that stubs will have more advantage over decoupling capacitors and stub on-chip integration will be possible in higher frequency operation LSIs.
2.7 Appendix

This section describes many equations associated with stubs, but it is optional. You can skip reading this section.

2.7.1 Capacitance Termination

When the stub is terminated by a capacitor $C_l$, the reflection coefficient becomes

$$\Gamma_l = \frac{1}{\frac{1}{j\omega C_l} - Z_0} = 1 \cdot e^{-j\theta} \quad (2.52)$$

using eqn(2.7). It shows that only phase rotation occurs without loss on the capacitance termination. The phase rotation can be compensated by shorten the stub length to $l - \Delta l$ such that

$$\beta, 2\Delta l = \theta \quad (2.53)$$

so as to be equivalent with a stub length $l$ with an open termination. Unfortunately, eqn(2.53) shows that $\Delta l$ depends on frequency.

This relation can be applied when the phase rotation occurs because of many reasons, such as $Z_0$ has an imaginary part based on the loss of the stub, or the termination impedance has a imaginary part. But again, both $\Delta l$ and $\theta$ depend on frequency.

2.7.2 Transient Analysis

Assuming that $I_0$ is a current source, a near end source impedance $Z_s$ and a stub whose characteristic impedance is $Z_0$ are connected in parallel. $I_{fn}$ and $I_{bn}$ are the forward- and backward- going waves at the stub near end. At the initial condition, the stub input impedance looks $Z_0$.

$$I_{fn}(t = 0) = \frac{Z_s}{Z_s + Z_0} I_0 = A I_0 \quad (2.54)$$

$$A = \frac{Z_s}{Z_s + Z_0} \quad (2.55)$$

$$I_{bn}(t = 0) = 0. \quad (2.56)$$

The round trip attenuation $B$ is

$$B = \eta e^{-j\theta/2}\Gamma_l. \quad (2.57)$$

The forward- and backward- going waves increase at every reflection, and become

$$I_{fn} = A I_0 + A I_0 \cdot B \Gamma_s + \cdots + A I_0 \cdot (B \Gamma_s)^{r-1}$$

$$I_{bn} = A I_0 B + A I_0 B \cdot (B \Gamma_s) + \cdots + A I_0 B \cdot (B \Gamma_s)^{r-1}$$

The current going through the source impedance $I_s$, and the stub $I_{stub}$ become

$$I_s = (1 - A)I_0 + (1 - \Gamma_s)I_{fn} \quad (2.60)$$

$$I_{stub} = I_{fn} - I_{bn} \quad (2.61)$$

where $\Gamma_s$ is the reflection coefficient at the near end. When the stub has an open termination ($\Gamma_s = 1$) and the stub length is quarter of the voltage wave ($\beta l = \pi/2$), the reflection occurs every $T/2 (=1/2f)$ period,

$$r \rightarrow \frac{T}{2} = 2ft \quad (2.62)$$

from eqn(2.57)

$$B = -\eta \quad (2.63)$$

from eqn(2.55),(2.63),(2.58)

$$I_{fn} = \frac{Z_s}{Z_s + Z_0} \cdot \frac{1 + \eta \Gamma_s (-\eta \Gamma_s)^{2ft}}{1 + \eta \Gamma_s} I_0 \quad (2.64)$$

$$= \frac{Z_s (1 + \eta \Gamma_s (-\eta \Gamma_s)^{2ft})}{(1 + \eta Z_s + (1 - \eta)Z_0)} I_0 \quad (2.65)$$

$$\rightarrow (1 + \eta)Z_s + (1 - \eta)Z_0 I_0 \quad [t \rightarrow \infty] \quad (2.66)$$

$$V_{fn} = Z_0 I_{fn} \quad (2.67)$$

from eqn(2.55),(2.63),(2.59)

$$I_{bn} = \frac{Z_s}{Z_s + Z_0} \cdot \frac{-\eta - \eta Z_s (1 - (-\eta \Gamma_s)^{2ft})}{1 + \eta \Gamma_s} I_0 \quad (2.68)$$

$$= \frac{-\eta Z_s (1 - (-\eta \Gamma_s)^{2ft})}{(1 + \eta Z_s + (1 - \eta)Z_0)} I_0 \quad (2.69)$$

$$\rightarrow (1 + \eta)Z_s + (1 - \eta)Z_0 I_0 \quad [t \rightarrow \infty] \quad (2.70)$$

$$V_{bn} = Z_0 I_{bn} \quad (2.71)$$

from eqn(2.55),eqn(2.60)

$$I_s = \frac{Z_0(I_0 + 2I_{bn})}{Z_s + Z_0} \quad (2.72)$$

$$\rightarrow \frac{(1 + \eta)Z_s}{(1 + \eta)Z_s + (1 - \eta)Z_0} I_0 \quad [t \rightarrow \infty] \quad (2.73)$$

$$V_s = Z_s I_s \quad (2.74)$$

$$\rightarrow Z_0 I_{fn} + Z_0 I_{bn} \quad (2.75)$$

$$I_{stub} = I_{fn} - I_{bn} \quad (2.76)$$

$$\rightarrow \frac{(1 + \eta)Z_s}{(1 + \eta)Z_s + (1 - \eta)Z_0} I_0 \quad [t \rightarrow \infty] \quad (2.77)$$

$$I_s + I_{stub} \rightarrow I_0 \quad [t \rightarrow \infty] \quad (2.78)$$

In order to know the time constant,

$$(-\eta \Gamma_s)^{2ft} = e^{2j/(\log|\eta\Gamma_s|)} \quad \text{[\text{Eqn. 2.79}]}$$

$$\log z = \log|z| + j \arg z \quad (2.80)$$

$$e^{2j/(\log|\eta\Gamma_s|)} \quad (2.81)$$

$$e^{2j/(\log|\eta\Gamma_s|)} \quad (2.82)$$

This equation shows that the time constant to become the steady state is

$$\tau = \frac{1}{-2f \log|\eta\Gamma_s|} \quad (2.83)$$
Note that $|\eta \Gamma| \leq 1$, and $\tau$ is positive.

The corresponding differential equations are derived as follows.

$$\frac{dI_{fn}}{dt} = CD'(D = B\Gamma_z) \quad (2.84)$$

$$I_{fn}(t = 0) = A \quad (2.85)$$

$$I_{fn}(t = 1) = A + AD. \quad (2.86)$$

Solve these equations,

$$\frac{dI_{fn}}{C} = D'dt \quad (2.87)$$

$$\frac{I_{fn}}{C} = \frac{1}{\log D} D' + E \quad (2.88)$$

$$I_{fn} = \frac{C}{\log D} \frac{1}{1 - D} + E = A + AD \quad (2.89)$$

When the stub has an open termination ($\Gamma_z = 1$) and the stub length is quarter of the voltage wave ($\beta l = \pi/2$), and adopt the equivalent termination impedance model,

$$I_{fz} = I_{f0}e^{-\beta z} \quad (2.107)$$

$$I_{bc} = -I_{f0}\Gamma_{Equiv} e^{\beta l} \quad (2.108)$$

$$I_z = I_{fz} - I_{bc} \quad (2.109)$$

$$= I_{f0}(e^{-\beta z} + \Gamma_{Equiv} e^{\beta l}) \quad (2.110)$$

$$V_z = Z_0 I_{fz} + Z_0 I_{bc} \quad (2.111)$$

$$= Z_0 I_{f0}(e^{-\beta z} - \Gamma_{Equiv} e^{\beta l}) \quad (2.112)$$

The voltage and the current at the near and the far end are

$$I_{zn} = I_{f0}(1 + \Gamma_{Equiv}) \quad (2.113)$$

$$I_{zf} = -j I_{f0}(1 - \Gamma_{Equiv}) \quad (2.114)$$

$$V_{zn} = Z_0 I_{f0}(1 - \Gamma_{Equiv}) \quad (2.115)$$

$$V_{zf} = -j Z_0 I_{f0}(1 + \Gamma_{Equiv}) \quad (2.116)$$

Substitute (2.66) and replace $\Gamma_{Equiv}$ with $\eta$ based on eqn(2.16), we will get

$$I_{zn} = \frac{(1 + \eta)Z_z}{(1 + \eta)Z_z + (1 - \eta)Z_0} I_0 \quad (2.117)$$

$$I_{zf} = \frac{j(1 - \eta)Z_z}{(1 + \eta)Z_z + (1 - \eta)Z_0} I_0 \quad (2.118)$$

$$V_{zn} = \frac{(1 - \eta)Z_z}{(1 + \eta)Z_z + (1 - \eta)Z_0} I_0 \quad (2.119)$$

$$V_{zf} = \frac{-j(1 + \eta)Z_z}{(1 + \eta)Z_z + (1 - \eta)Z_0} I_0 \quad (2.120)$$

When the stub has an open termination ($\Gamma_z = 1$) and the stub length is quarter of the voltage wave ($\beta l = \pi/2$), and if we do not use the equivalent termination impedance model,

$$I_{fz} = I_{f0}e^{-\alpha z} e^{-\beta z} \quad (2.121)$$

$$I_{bc} = -I_{f0}e^{\alpha(2l-\zeta)} e^{\beta l} \quad (2.122)$$

$$I_z = I_{fz} - I_{bc} \quad (2.123)$$

$$= I_{f0}(e^{\alpha z} e^{-\beta z} - e^{\alpha(2l-\zeta)} e^{\beta l}) \quad (2.124)$$

$$V_z = Z_0 I_{fz} + Z_0 I_{bc} \quad (2.125)$$

$$= Z_0 I_{f0}(e^{\alpha z} e^{\beta l} - e^{\alpha(2l-\zeta)} e^{\beta l}) \quad (2.126)$$

We can use the eqn(2.66), however, the equations will not be simple.

When no resistance on the stub (i.e. $\alpha = 0$),

$$I_{fz} = I_{f0}e^{-\beta z} \quad (2.127)$$

$$I_{bc} = -I_{f0}e^{\beta l} \quad (2.128)$$

$$I_z = I_{fz} - I_{bc} \quad (2.129)$$

$$= I_{f0}(e^{-\beta z} + e^{\beta l}) \quad (2.130)$$

$$= 2I_{f0} \cos(\beta l) \quad (2.131)$$

$$V_z = Z_0 I_{fz} + Z_0 I_{bc} \quad (2.132)$$

$$= Z_0 I_{f0}(e^{-\beta z} - e^{\beta l}) \quad (2.133)$$

$$= -2Z_0 I_{f0} \sin(\beta l) \quad (2.134)$$

2.7.3 I, V distribution along the stub

Assume that an incident wave $I_{f0}$ going into the stub and the stub length is $l$, the current and voltage at the point $z$ are

$$I_{fz} = I_{f0}e^{-\alpha z} e^{-\beta z} \quad (2.101)$$

$$I_{bc} = I_{f0}\Gamma z e^{\alpha(2l-\zeta)} e^{-\beta l} \quad (2.102)$$

$$I_z = I_{fz} - I_{bc} \quad (2.103)$$

$$= I_{f0}(e^{\alpha z} e^{-\beta z} - \Gamma z e^{\alpha(2l-\zeta)} e^{-\beta l}) \quad (2.104)$$

$$V_z = Z_0 I_{fz} + Z_0 I_{bc} \quad (2.105)$$

$$= Z_0 I_{f0}(e^{\alpha z} e^{-\beta z} + \Gamma z e^{\alpha(2l-\zeta)} e^{-\beta l}) \quad (2.106)$$

which is the same as eqn(2.64).
The stub does not consume power because the $I_z$ and $V_z$ has $\pi/2$ phase difference.

### 2.7.4 Voltage Transformers

Using eqn (2.117)-(2.120), the ratio of the near end and the far end by using the equivalent termination impedance model become

$$
\frac{V_{z,l}}{V_{z,0}} = \frac{1 + \eta}{1 - \eta}
$$

(2.135)

$$
\frac{I_{z,l}}{I_{z,0}} = \frac{1 - \eta}{1 + \eta}
$$

(2.136)

### 2.7.5 Q factor

Here, the stub is replaced with series connected $R_{eq}, L_{eq}, C_{eq}$ lump elements terminated to GND, around the resonant frequency $f_0$.

$$
Z = R_{eq} + j(\omega L_{eq} - \frac{1}{\omega C_{eq}})
$$

(2.137)

$$
Z = R_{eq} + j\left(\frac{d}{d\omega}(\omega L_{eq} - \frac{1}{\omega C_{eq}})\right)_{\omega=\omega_0}
$$

(2.138)

$$
Z = R_{eq} + j (L_{eq} + \frac{1}{\omega^2 C_{eq}}) \Delta \omega
$$

(2.139)

$$
|Z|^2 = \frac{R_{eq}^2}{2L_{eq}}
$$

(2.142)

$$
\Delta \omega_{BW} = \frac{R_{eq}}{2T_{eq}}
$$

(2.143)

The definition of Q is

$$
Q = \frac{R_{eq}}{2\Delta \omega_{BW}}
$$

(2.144)

$$
Q = \frac{\omega_0}{2R_{eq}}
$$

(2.145)

$$
Q = \frac{\omega_0 L_{eq}}{R_{eq}}
$$

(2.146)

$$
Q = \frac{\sqrt{L_{eq} C_{eq}}}{R_{eq}}
$$

(2.147)

$$
Q = \frac{1}{\sqrt{L_{eq} C_{eq}}}
$$

(2.148)

Thus, from eqn (2.141), $Z$ becomes

$$
Z = R_{eq}(1 + \frac{2L_{eq} \Delta \omega}{R_{eq}})
$$

(2.149)

$$
= R_{eq}(1 + \frac{2}{R_{eq}} \sqrt{\frac{L_{eq}}{C_{eq}}} \sqrt{L_{eq} C_{eq} \Delta \omega})
$$

(2.150)

From eqn (2.9), the stub input impedance with an open termination is

$$
Z_{stub} = \frac{1}{j\tan \beta l}
$$

(2.151)

When the stub length is quarter of the wavelength,

$$
\beta l = \frac{\omega}{c} \cdot \frac{c}{\omega_0/2\pi}
$$

(2.152)

$$
\approx \frac{\pi}{2} \cdot \frac{\omega_0}{\omega_0}
$$

(2.153)

$$
\approx \frac{\pi}{2} \cdot (1 + \frac{\Delta \omega}{\omega_0}).
$$

(2.154)

Then,

$$
Z_{stub} = Z_0 \frac{1}{2 \tan(\alpha l + j\frac{\pi}{2})}
$$

(2.155)

$$
= Z_0 \frac{1}{\tan(\alpha l + j\frac{\pi}{2} \frac{\Delta \omega}{\omega_0} + j\frac{\pi}{2})}
$$

(2.156)

$$
[tan(z) + j\frac{\pi}{2} \frac{\Delta \omega}{\omega_0}]
$$

(2.157)

$$
= Z_0 \frac{1}{\tan(\alpha l \frac{\Delta \omega}{\omega_0})}
$$

(2.158)

$$
= Z_0 \frac{1}{\tan(\alpha l \frac{\Delta \omega}{\omega_0})}
$$

(2.159)

$$
= Z_0 \frac{\Delta \omega}{\omega_0}.
$$

(2.160)

Here, $\gamma$ of eqn (2.3) becomes

$$
\gamma = \frac{\omega_0}{2} + j \omega \sqrt{LC} \equiv \alpha + j \beta,
$$

(2.161)

where $R \approx \omega L$ and $G \approx \omega C$, so that

$$
\alpha = \frac{R}{\omega_0} + G \omega_0
$$

(2.162)

$$
= \frac{\pi}{2} \frac{\Delta \omega}{\omega_0}
$$

(2.163)

$$
= \frac{\pi}{2} \left(\frac{\Delta \omega}{\omega_0}\right)
$$

(2.164)

$$
[tan(z) + j\frac{\pi}{2} \frac{\Delta \omega}{\omega_0}]
$$

(2.165)

$$
= Z_0 \left(\tanh(\alpha l + j\frac{\pi}{2} \frac{\Delta \omega}{\omega_0})\right)
$$

(2.166)

$$
= Z_0 \left(\tanh(\alpha l \frac{\Delta \omega}{\omega_0})\right)
$$

(2.167)

$$
= Z_0 \left(\alpha \frac{\pi}{2} \frac{\Delta \omega}{\omega_0} \right)
$$

(2.168)

When $R \approx \omega L$ and $G \approx \omega C$, so that

$$
\alpha = \frac{R}{\omega_0} + G \omega_0
$$

(2.169)

$$
\beta = \omega \sqrt{LC}.
$$

(2.170)
Compare eqn(2.168) with (2.151),

$$Q = \frac{\beta_0}{2\alpha} = \frac{\omega_0 \sqrt{LC}}{2 \left( \frac{R}{Z_0} + \frac{GW^2}{G^4} \right)}$$

$$= \frac{\omega_0 Z_0 \sqrt{LC}}{R + GZ^2_0} = \frac{\omega_0 \sqrt{L \omega^2_0 - VT}}{R + GZ^2_0}$$

$$= \frac{\omega_0 L}{R + GL/C}$$

$$R_{eq} = \frac{\pi Z_0 \alpha}{2} = \frac{\pi Z_0}{2Q}$$

$$Z_{stub} = R_{eq}(1 + jQ \frac{2\Delta\omega}{\omega_0})$$

Here, the frequency dependency are

$$Q = \frac{\omega_0 L}{R + GL/C} \quad [\text{const to } f_0]$$

$$\Delta\omega_{BW} = \frac{\omega_0}{2Q} = \frac{(R + GL/C)}{2L}$$

$$R_{eq} = \frac{R + GL/C}{\frac{\pi}{2} \frac{\omega_0}{\sqrt{LC}}} \quad [\text{const to } f_0]$$

$$R_{eq}$$ is the stub input impedance when open termination and the stub length is quarter of the voltage wave, which should be equal to eqn(2.17) and eqn(2.27). Numerical calculation give similar results.

Then, the stub can be corresponded with the lump $R_{eq}, L_{eq}, C_{eq}$ around the resonant frequency.

$$R_{eq} = \frac{\pi Z_0}{4Q} \quad [\text{from eqn(2.175)}]$$

$$= \frac{\pi}{4} \sqrt{\frac{LC}{\omega_0 L}} \quad [\text{from eqn(2.174)}]$$

$$= \frac{L}{2} \cdot \lambda_0 \quad \frac{2}{4}$$

$$L_{eq} = \frac{R_{eq} Q}{\omega_0} \quad [\text{from eqn(2.146)}]$$

$$= \frac{\pi Z_0}{4Q} \quad [\text{from eqn(2.175)}]$$

$$= \frac{\pi}{4} \frac{\omega_0 L}{\omega_0 \sqrt{LC}} \quad \sqrt{\frac{L}{C}}$$

$$= \frac{L}{2} \cdot \lambda_0 \quad \frac{2}{4}$$

$$C_{eq} = \frac{1}{\omega_0^2 L_{eq}} \quad [\text{from eqn(2.181)}]$$

$$= \frac{4 \sqrt{LC}}{\pi^2 \omega_0^2 \sqrt{C}} \quad \sqrt{\frac{C}{L}}$$

$$= \frac{8 \sqrt{LC}}{\pi^2 \omega_0^2 \sqrt{C}} \quad \frac{\lambda_0}{4}$$

Note that

$$Z_0 = \sqrt{\frac{L}{C}} \neq \sqrt{\frac{L_{eq}}{C_{eq}}} = \frac{\pi}{4} Z_0$$

and

$$\omega_0 = \frac{1}{\sqrt{L_{eq} C_{eq}}} = \sqrt{\frac{\pi^2}{4 \sqrt{LC}}} \neq \frac{1}{\sqrt{LC}}.$$
Chapter 3

Experiments for Power Supply Noise Reduction using Stubs

Abstract

This chapter demonstrates power supply noise reduction using stubs. A quarter-length stub attached to the power supply line of an LSI chip works as a band-eliminate filter, and suppresses the power supply noise of the designed frequency. Although the on-chip stub does not show the noise reduction effects mainly because the stub parasitic resistance is too big as well as the stub is bent inside the chip and reflections occur, on-board stubs and off-chip stubs clearly reduce the power supply noise as theoretically predicted in the previous chapter. The measurement results show that 87% of the designed frequency noise component and 39% of the total noise are reduced when the stub patterns are written on a power supply area on a PCB board for a 1.25GHz operating LSI, and 90% of the designed frequency noise component and 48% of the total noise are reduced when the off-chip stubs are attached to the 1.15GHz operating test chip, respectively. These results also show the possibility of the stub on-chip integration which can eliminate the package and bonding wire parasitic impedance effects when the chip operating frequency becomes higher and the stub length becomes shorter.
3.1 Introduction

It is theoretically shown in the previous chapter that stubs are more efficient on some cases than decoupling capacitors for power supply noise and $di/dt$ reduction. This chapter shows experimental results of the stub power supply noise reduction effects.

Measurement results of an on-chip stub for the power supply noise reduction is shown in Sect.3.2. Section 3.3 and Sect.3.4 describe setups and measurements of on-board and off-chip stubs noise reduction, respectively. Discussions are given in Sect.3.5, and Sect.3.6 summarizes this chapter.

3.2 On-chip Stubs

3.2.1 Stub Design

We use 0.18µm 5ML standard CMOS technology, and the target frequency is set to 2.5GHz. The designed stub structure is shown in Fig.3.1. ML5 and ML4 are tied together to reduce the resistance of the power line, and ML1 plane is used for the ground. The stub width is set to 40µm. The inductance $L=102nH/m$ and the capacitance $C=407pF/m$ are extracted by Raphael[10] 2D field solver, and the resistance $R=500Ω/m$ is calculated based on the sheet resistance value provided from the fab. As well as the stub for the target frequency, 2.5GHz, a stub for the second harmonic 5GHz is designed since it is the second dominant frequency of the noise as shown in Fig.2.10(b). The stub length for 2.5GHz and 5GHz is 15.323mm and 7.662mm, respectively. The same-area decoupling capacitor shown in Fig.3.2 is also designed using ML5 and ML4 together for Vdd and ML1 for Gnd plane.

3.2.2 Test Circuit

A PRBS (Pseudo Random Bit Stream) $2^7 - 1$ generation circuit with an inverter chain at each output of the DFFs is used as our test circuit, as shown in Fig.3.3. This circuit represents common synchronous circuits. The PRBS pattern and the inverter chains represent random switching of LSIs and the combination logics, respectively. The length of the inverter chains distributes from 2 to 12, which represents a path length distribution between DFFs.

The test circuit contains VCO so that we can easily sweep the operating frequency by changing the DC control voltage ($Vctrl$). The selector circuit selects the random mode which use the feedback from the XOR gate, or the repeat mode which use the $CLK/2$ signal, to the input of the shift register. The repeat mode is the optimistic case and the
Figure 3.1: Stub structure. $R = 500\, \Omega/m$, $L = 102\, nH/m$, $C = 407\, pF/m$, $G = 0$.

Figure 3.2: Designed stub and the same-area decoupling capacitor structures.
Figure 3.3: Internal circuit. A PRBS generator and inverter chains. The selector selects the repeat mode or the random mode.

Figure 3.4: Four types of power line structures.
random mode is the pessimistic case from the stub noise reduction point of view.

Four types of power line structures as shown in Fig.3.4 are designed and fabricated: The stubs for 2.5GHz and 5GHz together, the stub for 2.5GHz, the same-area decoupling capacitor, and nothing.

### 3.2.3 Setups

The test chip was designed and fabricated using 0.18µm 5ML standard CMOS technology, and the chip size is 5.9mm×5.9mm, as shown in Fig.3.5.

The chip is mounted on a Cu board as shown in Fig.3.6. The DC bias of $V_{dd_{internal}}$, $V_{dd_{io}}$, $V_{ctrl}$ and $SEL$ are supplied through lead lines to the “islands” on the board. The voltage of the islands are stabilized by several chip capacitors. The surface of the chip is covered with shield tape. The high-speed output signals are $CLK/32$ which is used as a trigger for a oscilloscope, $PRBS$ and virtual$V_{dd}$ node. The 50Ω transmission lines are directly connected to the output pins to reduce reflections.

![Figure 3.5: Chip Photograph. 0.18µm 5ML CMOS, 5.9mm×5.9mm.](image-url)
3.2.4 Measurement Results

Four types of power supply noise, with the stubs for 2.5GHz and 5GHz, the stub for 2.5GHz, the decoupling capacitor, the nothing, are measured and compared. The chip is under the repeat mode on the measurement because the waveforms cannot be observed by a sampling oscilloscope under the random mode.

Figure 3.7 shows the VCO control voltage dependence of the clock frequency and the average voltage of the internal power supply node. The frequency rises as the VCO voltage becomes higher, and the average power supply voltage decreases because of the IR drop. Since the four lines are overlapped each other, noise characteristic differences shown in the followings are caused by the power supply line difference instead of the intra-chip fluctuations.

The measured power supply noise waveforms and the corresponding spectrum are shown in Fig.3.8 and Fig.3.9. The VCO control voltage is 2.8V and the operating frequency is 2.33GHz. The difference of the nothing, the decoupling capacitor and the stub is not clear. And the noise spectrum have the peaks at 1/2 and 1/4 operating frequency.

In order to investigate the reasons, we changes the IO supply voltage with keeping the constant voltage for the internal circuit and the VCO. The measured noise spectrum
Figure 3.7: VCO characteristics and IR drop.

Figure 3.8: Measured virtualVdd voltage of the nothing, capacitor and stub case.
Figure 3.9: Measured virtual\(V_{dd}\) noise spectrum of the nothing, capacitor and stub case.

Figure 3.10: Noise spectrum change of the IO supply voltage.
is shown in Fig. 3.10. Since the VCO control voltage is constant, the operating frequency does not change. The spectrum amplitude of the operating frequency component are the same while \( f/2 \) and \( f/4 \) components depend on the IO supply voltage. Therefore, we can say that these \( f/2 \) and \( f/4 \) components are caused by the IO buffer switching noise. The power line are designed such that the power rail for the internal circuit and for the IO buffer are isolated. However, the IO buffer switching noise is coupled to the internal power line via the substrate or the package.

Figure 3.11 shows the operating frequency dependence of the internal power supply noise of the operating frequency component. The noise amplitude decreases as the operating frequency increases. This is because the resonant frequency of the internal parasitic capacitors, such as well junction capacitors and source junction capacitors, with the parasitic inductance of the package are lower than the operating frequency, and AC currents are provided from the parasitic capacitors at the frequency which is higher than the resonant frequency.

The noise amplitude difference of the four types of power line structures are not clear. This is because

- The stubs are bent in the chip, and the reflection occurs there. Thus the equivalent stub length differs from \( \lambda/4 \).

![Figure 3.11: Operating frequency vs. operating frequency component of the virtualVdd noise with the nothing, capacitor and stub case.](image-url)
• The resistance is much bigger than the estimated value especially if the skin effects are taken into consideration. The fab.-provided resistance value seems to be a measured sheet resistance with a DC signal.

• The package impedance is so big that the internal parasitic capacitors works, and the noise signal cannot come out from the package.

Here, the stub effects cannot be observed at this operating frequency if the stub is fabricated on-chip. Thus, on-board stubs are investigated in the next section.

3.3 On-board Stubs

3.3.1 Setups

We use the same internal test circuit as Fig.3.3, and the test circuit was fabricated on a smaller test chip (2.8mm×2.8mm) as shown in Fig.3.12 in order to use a smaller package whose parasitic impedance is also smaller. Three types of power line test structures are fabricated in the same chip, however, only “nothing” type is used for the on-board stub experiments.

The chip is mounted on a Cu board as shown in Fig.3.13, and the corresponding schematic is shown in Fig.3.14. The DC bias of $V_{dd}$, $V_{ddio}$, $V_{ctrl}$ and $SEL$ are supplied through lead lines to the islands on the board. The voltage of the islands are stabilized by several chip capacitors. The $V_{ddn}$ island which is the power supply for the internal circuit is connected to the $V_{dd}$ island by a wire and has no chip capacitor. The parasitic inductance of the wire causes noise voltage to the $V_{ddn}$ island.

Two types of the $V_{ddn}$ island has been tested. One is “without stubs” which is 4.7mm×10.0mm rectangle, the other is “with stubs” which has 1.25GHz and 1.95GHz stubs attached to the “without stubs” rectangle. The voltage of the $V_{ddn}$ island is directly probed by 50Ω transmission line so that the power supply noise can be measured by the spectrum analyzer and the oscilloscope. Other 50Ω transmission lines are also connected to the $CLK/32$ and $PRBS$ output pins of the test chip, and connected to the oscilloscope.

3.3.2 Stub Design

The stubs are adjusted around 1.25GHz and 1.95GHz in our experiment. The stub patterns are written on the surface of the PCB board whose dielectric material is 1mm thickness FR4 ($\epsilon_r=4.8$) sandwiched by 18µm copper films. The stubs are composed of microstrip
Figure 3.12: Chip photograph. 0.18\(\mu\)m 5ML CMOS, 2.8mm\(\times\)2.8mm.
Figure 3.13: Photograph of the chip mount, (a) without stubs, and (b) with stubs.

Figure 3.14: Schematic of the measurement setup.
line with the width of 1mm, and the effective dielectric constant becomes [14]

\[
\epsilon_{\text{eff}} = \frac{\epsilon_r + \frac{1}{2}}{2} + \frac{\epsilon_r - 1}{2} \left( 1 + \frac{12h}{w} \right) = 3.427
\]  

(3.1)

if only the cupper film is removed. However, the stub patterns are written by scratching the FR4 with dozens of micron meter depth as well as the cupper film and hence the effective dielectric constant becomes smaller. Another reason is edge effects. Chapter 2 assumes that \( L, C \) are constant along the stub with an open termination, however, the actual \( L, C \) values become different around the stub edges, also the termination is not completely open. By accounting these issues, the effective dielectric constant for eqn(2.10) becomes 2.66 in our case, and the stub length are 36.7mm and 23.5mm for 1.25GHz and 1.95GHz, respectively.

3.3.3 S-parameter

Figure 3.15 shows the transmission characteristics (\( S_{21} \)) of \( Vddn \) island of the with/without stubs, measured by a network analyzer. It is shown that the signals around 1.25GHz and 1.95GHz are absorbed by the stubs.

![Figure 3.15: \( |S_{21}| \) of the with/without stubs case.](image)
3.3.4 Noise Spectrum

Figure 3.16 shows the measured spectrum of the power supply noise of the random mode at the 1.25GHz operation with/without the stubs. This graph shows that the dominant noise frequency is the operating frequency, and spread around it because of its PRBS pattern. The stub suppresses the noise around 1.25GHz.

The measured waveforms of the Vddn island on the random mode is shown in Fig.3.17. It is shown that the power supply noise is reduced by the stub. However, the noise of the random mode cannot be completely suppressed because of the lower frequency component which the stubs cannot suppress, as shown in Fig.3.16.

Figure 3.16: Measured spectrum of the random mode at 1.25GHz operation of the with/without stubs cases. (i-b) The spectrum of the lower frequency.
3.3.5 Operating Frequency Dependence of the Noise Amplitude

The operating frequency dependence of the measured spectrum of the random mode is shown in Fig.3.18. When the operating frequency and the stub frequency match in (i) and (iv), the spectrum have different peak amplitudes for with/without stubs. When the operating frequency does not match with the stub frequency, the spectrum are similar for with/without stubs. Figure 3.19(a) shows the operating frequency dependence of the noise amplitude of the operating frequency component, and Fig.3.19(b) shows the operating frequency dependence of the total noise, with the line of the (i)-(v) frequencies. The total noise value here is defined by the standard deviation $\sigma$ from the average voltage $V_{av}$,

$$V_{av} = \frac{1}{N} \sum_{i=1}^{N} V_i, \quad \sigma = \sqrt{\frac{1}{N-1} \sum_{i=1}^{N} (V_i - V_{av})^2}$$  \hspace{1cm} (3.2)

where $N$ is the number of the sampling points which is 4096, and the sampling time step is constant in this experiment, as shown in Fig.3.17.

The graph (a) indicates that the stubs for 1.25GHz, 1.95GHz remove 87%, 72% of the designed frequency noise, in case (i), (iv), respectively. The total noise reduction ratio of with/without stubs are 39% in case (i) and 19% in case (iv), as shown in Fig.3.19(b).
Figure 3.18: Operating frequency dependence of the random mode spectrum, with/without the on-board stubs.
Figure 3.19: Operating frequency dependence of the power supply noise in the random mode, with/without the on-board stubs. (a) Noise amplitude of the operating frequency component. (b) Total noise amplitude.
3.3.6 Lower Frequency Noise

As shown in Fig.3.16(i-b), the power supply noise spectrum have some amount of power in lower frequency components. The PRBS $2^7 - 1$ circuit generates pseudo-random bit pattern which repeats in every $2^7 - 1 = 127$ clock cycles, and the stream has $1.25GHz/127 = 9.84MHz$ component as the basic frequency at the $1.25GHz$ operation. Figure 3.16(i-b) shows that the lower frequency set are the harmonics of the basic frequency. It means that these noises are caused by the PRBS $2^7 - 1$ stream characteristics.

3.3.7 Current Distribution along the Stubs

When a noise frequency matches with a stub frequency, the current and the voltage distribution along the stub are

$$|I(z)| = A \cos(\beta z), \quad |V(z)| = -jZ_0 A \sin(\beta z)$$  (3.3)

as being derived at eqn(2.131) and (2.134), where $A$ is a constant value, $\beta$ is the phase constant and $z$ is the location of the stub.

The current distribution along the stubs are measured by using a magnetic probe[15] which picks up the magnetic field caused by the current and measures the induced voltage by the spectrum analyzer, as shown in Fig.3.20. The current was measured at ten points for each stub when the operating frequency is $1.25GHz/1.95GHz$ for the $1.25GHz/1.95GHz$ stubs, respectively, and the results are shown in Fig.3.21 with the ideal distribution given by eqn(3.3). Since the magnetic probe has frequency dependence between the current and the induced voltage amplitude, the graph shows the normalized current value for each stub. The measured and theoretical current distribution have same tendency, and showing that the stubs work for the power supply noise reduction of the designed frequency.

3.3.8 Operating Frequency Dependence

As being discussed in the previous section, the stubs remove the noise of the designed frequencies. In case (iii), however, the noise amplitude of the operating frequency is suppressed even though the frequency is not the frequencies of the stubs, as shown in Fig.3.18(iii) and Fig.3.19(a). This is because of the package and bonding wire frequency characteristics. The transistor switchings occur inside the LSI package, and the impedance of the package and bonding wire is large enough at the frequency that the noise does not come out from the package. Thus, the noise of the frequency is not observed.
Figure 3.20: Current measurement using a magnetic probe. The circles and the squares indicate the measured points.

Figure 3.21: Normalized current distribution along the stubs. The markers are measurement results, and the dashed lines are ideal curves given by eqn(3.3).
3.4 Off-chip Stubs

3.4.1 Setups

Off-chip stubs are also implemented and tested. Here, we use the same chip as the “without stubs” case in the previous section, and put the stub wires as shown in Fig.3.22.

![Figure 3.22: Photograph of the chip mount and the off-chip stubs.](image)

3.4.2 Stub Design

The diameter of the stub wire is about 1mm. The one edge of the stubs are soldered to the $V_{ddn}$ island, and the rest of the part stay in the air with the height of about 1mm from the board. In this experiment, the stubs are adjusted for 1.15GHz and 1.80GHz whose stub length are 6.52cm and 4.17cm, respectively, according to eqn(2.10) since the relative dielectric constant of the air is 1.

The stubs are easily removed so that we can compare the measurement results with/without the stubs.
3.4.3 Measurement

The operating frequency dependence of the spectrum is shown in Fig.3.23 and the noise amplitude are shown in Fig.3.24. These graphs show that the off-chip stubs have very

Figure 3.23: Operating frequency dependence of the random mode spectrum, with/without the off-chip stubs.
similar characteristics to the on-board stubs, as being compared with Fig.3.18 and Fig.3.19. The off-chip stubs for 1.15GHz, 1.80GHz remove 90%, 84% of the designed frequency noise, and remove 48%, 15% of the total noise, respectively.

Figure 3.24: Operating frequency dependence of the power supply noise in the random mode, with/without the off-chip stubs. (a) Noise amplitude of the operating frequency component. (b) Total noise amplitude.
3.5 Discussion

3.5.1 Possibility of On-chip Stub

Stub length is in inverse proportion to the operating frequency, as expressed by eqn(2.10), and the dielectric constant becomes 3.9 if the stubs are integrated on-chips because the stubs stay in SiO₂. Figure 3.25 shows the prediction of the required stub length based on the ITRS roadmap of MPU clock frequency[1]. It shows that the stub length will be shortened to about 5mm in 2007, and on-chip stubs will be possible.

![Figure 3.25: ITRS roadmap of MPU clock frequency, and corresponding stub length.](image)

3.6 Summary

This chapter demonstrated power supply noise reduction using stubs. A quarter-length stub attached to the power supply line of an LSI chip works as a band-eliminate filter, and suppresses the power supply noise of the designed frequency. Although the on-chip stub does not show the noise reduction effects mainly because the stub parasitic resistance is too big as well as the stub is bent inside the chip and reflections occur, the on-board stubs and off-chip stubs clearly reduce the power supply noise as theoretically predicted in the previous chapter.
The measurement results show that 87% of the designed frequency noise component and 39% of the total noise are reduced when the stub patterns are written on a power supply area on a PCB board for a 1.25GHz operating LSI, and 90% of the designed frequency noise component and 48% of the total noise are reduced when the off-chip stubs are attached to the 1.15GHz operating test chip, respectively.

These results also show the possibility of the stub on-chip integration which can eliminate the package and bonding wire parasitic impedance effects when the chip operating frequency becomes higher and the stub length becomes shorter.
Chapter 4

An On-chip di/dt Detector for Power Supply

Abstract

This chapter demonstrates an on-chip di/dt detector. The di/dt detector consists of a power supply line, an underlying spiral inductor and an amplifier. The mutual inductor induces a di/dt proportional voltage, and the amplifier amplifies and outputs the value. The measurement results show that the di/dt detector output and the voltage difference between resistor terminals have good agreement. The di/dt reduction by a decoupling capacitor is also measured using the di/dt detector.
4.1 Introduction

Power supply noise is caused by the power line impedance and the power supply current. Along with IR drop, \(di/dt\) noise caused by the power line impedance and the current change \((di/dt)\) is becoming critical as the chip operating frequency advances. In addition, stricter electromagnetic compatibility (EMC) regulations have been enforced recently[2]. The dominant electromagnetic interference (EMI) noise is radiation from the power line of an LSI, and the EMI radiation is caused by \(di/dt\), not by voltage perturbation. Therefore, the \(di/dt\) analysis is important for EMI analysis as well as power supply noise analysis.

Many techniques have been proposed to measure power supply voltage bounce[16][17]. On the other hand, only few techniques have been developed for power supply current measurements. One technique uses a resistor connected in series to a power supply line on a PCB board and measures the voltage difference of the both terminals using electron-beam probing[18]. This technique needs numerical calculation to obtain the current and the \(di/dt\) waveforms. Another technique picks up the magnetic field caused by the current and measure the spectrum[15]. It is unable to reproduce the original current nor \(di/dt\) waveforms from the spectrum because the phase information is lost.

This chapter demonstrates an on-chip \(di/dt\) detector.

The \(di/dt\) detector is useful not only for a measure of \(di/dt\) for power supply noise and EMI noise analysis, but also it can be applicable for an automatic \(di/dt\) control since the detector is realized on-chip and outputs the \(di/dt\) value in real time.

In Sect.4.2, the basic concept and the circuit design of the \(di/dt\) detector are presented. Section 4.3 analyzes and gives necessary equations of the \(di/dt\) detector. Measurement results and discussions are described in Sect.4.4 and 4.5, then Sect.4.6 explains an improved version of the \(di/dt\) detector and Sect.4.7 introduces a feedback \(di/dt\) control circuit. Then Sect.4.8 summarizes this chapter.

4.2 Circuit Design

4.2.1 Basic Concept

Figure 4.1 shows the block diagram of the \(di/dt\) detector. A power supply current for the internal circuit goes through the power supply line inductance \(L_1\). A pickup inductance \(L_2\) coupled to \(L_1\) with a coupling coefficient \(K\) induces a \(di/dt\) proportional voltage. A noise-tolerant amplifier amplifies the induced voltage and outputs to a 50Ω transmission line that enables a high frequency measurement.
Figure 4.1: Block diagram of the $di/dt$ detector. The bold lines represent outside devices.

4.2.2 Mutual Inductance

The inductance $L_1$ should be small since it is in series connection to the power supply line. The small inductance requires a high coupling coefficient $K$ and a bigger $L_2$ in order to generate an enough induced voltage on the terminal of $L_2$.

The mutual inductor consists of the power supply line and an underlying spiral inductor. The power supply line $L_1$ is composed of the top metal layer ML3 with 1 turn, 20$\mu$m width. The spiral inductor $L_2$ has 10 turns with 2$\mu$m width and 2$\mu$m spacing using ML1. The outside diameter of the both inductors are 140$\mu$m $\times$ 140$\mu$m, as shown in Fig.4.2. This structure is called small mutual inductor. Another type of inductors, called large mutual inductor, has 200$\mu$m diameter and 24 turns.

The equivalent circuit of this mutual inductor structure is extracted by FastHenry[11] as shown in Fig.4.3.

4.2.3 Amplifier and Output Buffer

Since the output $di/dt$ value is a high speed analog signal, a high frequency and high linearity amplification with noise immunity is the key issue for the amplifier design.

The amplifier schematic is shown in Fig.4.4. We employ a current mirror type amplifier without current source. The resistors $R_b$ are used to keep the DC bias voltage as half-Vdd. The resistance is big enough to be considered open for AC signal. The bias condition realizes the maximum gain and the widest linearity for the amplifier.

We did not use a feedback type amplifier because it cannot respond to the high fre-
Figure 4.2: Mutual inductor structure.

Figure 4.3: Equivalent circuit of the small mutual inductor.
Figure 4.4: Amplifier/Output buffer, and measurement setup.

Frequency signals. Moreover, the $50\Omega$ load is too small to keep the linearity of the amplifier gain if the feedback amplifier is employed.

The output is connected to a transmission line whose characteristic impedance is $50\Omega$. The blocking capacitor $C_b$ is inserted at the input port of the oscilloscope to prevent the bias point change of the node $n_2$ due to the $50\Omega$ termination resistor connected to GND. Note that the average of the $di/dt$ value is zero because the current value is finite, and hence the blocking capacitor does not affect the $di/dt$ measurement.

The bias point of the amplifier is decided by the I-V characteristics of MN1, MN2, MP1, MP2 and the termination resistor $R_t$. The simulated I-V curves are shown in Fig.4.5 solid lines where the input voltage for MN1 and MN2 is half-vdd. The dashed lines show the bias point change when the input voltage for MN1 is half-vdd plus 0.1V and for MN2 is half-vdd minus 0.1V. The bias point of node $n_1$ moves from A to B, and the bias point of node $n_2$ moves from A to C. Assuming that the amount of the I-V curves change is linear,
Figure 4.5: I-V characteristics and the bias point.

Figure 4.6: Bias point change.
as shown in Fig.4.6, the following equation holds for the bias point B,

\[ g_{mn} \Delta V_{in} - g_{dsn} \Delta V_d = (g_{mp} + g_{dsp}) \Delta V_d \quad (4.1) \]

and the following equation holds for the bias point C,

\[ (g_r + g_{dsn}) \Delta V_{out} - g_{mn} \Delta V_{in} = (g_{mp} + g_{dsp}) \Delta V_d - g_{dsp}(\Delta V_d + \Delta V_{out}) \quad (4.2) \]

where \( g_{mn}, g_{mp} \) are the transconductance \( \partial I_d/\partial V_g \), and \( g_{dsn}, g_{dsp} \) are drain-source transconductance \( \partial I_d/\partial V_{ds} \) for NMOS and PMOS, respectively, and \( g_r \) is the conductance of the termination resistor. From these equations, the gain \( G \) is expressed as

\[ G = \frac{\Delta V_{out}}{2 \Delta V_{in}} = \frac{1}{2(g_{dsn} + g_{dsp} + g_r)} \left( g_{mn} + g_{mp} \right) \left( g_{mn} \right) \]

\[ \left( g_{mp} + g_{dsp} + g_{dsn} \right) \]

(4.3)

If no termination resistor is connected \((R_t = \infty \) or \( g_r = 0)\), the gain becomes bigger, the bias point easily go out from the saturation region and eqn(4.3) does not hold. However, the gain is limited by the smaller resistance, bigger \( g_r \) in eqn(4.3), so that the bias points stay within the saturation region.

According to HSPICE simulations, the gain of the amplifier \( G \) is 0.39, the cut-off frequency is 2.2GHz when no load capacitance, and the output linearity range is about \( \pm 0.35V \), with the single amplifier structure. Note that the open loop gain of this amplifier is 7.55, and the common mode rejection ratio (CMRR) is 2.34.

Though the single amplifier structure is employed here because the characteristics of the amplifier is enough for our purpose, it can be improved by using the dual amplifiers with plus-minus exchanged inputs and measure the difference of the output, as shown in Fig.4.4 “optional”. We can eliminate asymmetric characteristics and unexpected common-mode noises, and also increase the linear operation range and the gain, with this structure.

### 4.2.4 Internal Circuit as Noise Source

The internal circuit is shown in Fig.4.7. \( Vctrl \) changes the operating frequency through the VCO. The 1/2 divider and the 1/16 divider generate \( CLK/2 \) signal which is the input for the DFF chain, and \( CLK/32 \) signal which is used as a trigger for the oscilloscope. Each DFF has an inverter chain whose switching is the source of the \( di/dt \). The length of the inverter chains are distributed from 2 to 12. The delay of the longest inverter chain is 0.625ns. \( allORhalf \) signal controls the activation ratio of the circuit.

### 4.2.5 Power Supply Line Structures

The power supply line has an on-chip resistor \( R_i \) in series, the both terminals of which are connected to output pins to enable the current measurement by calculating the voltage dif-
ference, and compare the result with the $di/dt$ detector output as a reference. As shown in Fig. 4.8, the internal current goes out from $Vdd$ to the internal circuit through the package and bonding wire impedance $Z_{package}$, the series resistor $R_s$, and the inductor $L_1$.

Four types of circuits were designed. TypeA: no decoupling capacitor with the small mutual inductor, TypeB: the on-chip decoupling capacitor $C_d$ at the node after the detector with the small mutual inductor, TypeC: the on-chip decoupling capacitor at the node before the detector with the small mutual inductor, TypeD: no decoupling capacitor with the large mutual inductor.

### 4.2.6 Overview

The internal circuit switching causes the $di/dt$ which induces the voltage at the spiral inductor $L_2$ by the inductive coupling $K$. The amplifier amplifies and outputs the voltage to $didtOut$. The both terminals of the series resistor $R_s$ are connected to the oscilloscope as $s1$, $s2$ signals. Since the input voltage $Vctrl$ and $allORhalf$ are DC signals, no need to care
Figure 4.8: Over-all circuit with the measurement setup.
the high-speed characteristics for them. CLK/2 and CLK/32 signals come out through output buffers whose supply voltage is $V_{dd,i/o}$ which is neglected in the figure for simplicity. CLK/2 signal is used to check if the circuit works fine, CLK/32 is used as a trigger for the oscilloscope.

### 4.3 Analytical Models

#### 4.3.1 Equations

The mutual inductance $M$ is

$$M = K \sqrt{L_1 L_2}.$$  \hfill (4.4)

Assuming that the input current of the amplifier is $I_2$, the output voltage of the mutual inductor $V_2$ is

$$V_2 = M \frac{dI_i}{dt} + R_2 I_2 + L_2 \frac{dI_2}{dt} \approx M \frac{dI_i}{dt}.$$  \hfill (4.5)

Here $I_2$ is small enough because the input impedance of the amplifier is large enough compared with $R_2$ and $\omega L_2 (\omega \ll 10\text{GHz})$.

Assuming that the gain of the amplifier is $G$, the output voltage $V_{didt\text{Out}}$ of the $di/dt$ detector circuit is

$$V_{didt\text{Out}} = GV_2 = GK \sqrt{L_1 L_2} \frac{dI_i}{dt}$$  \hfill (4.6)

which means

$$\frac{dI_i}{dt} = \frac{1}{GK \sqrt{L_1 L_2}} V_{didt\text{Out}} \equiv A_{v2\text{didt}} V_{didt\text{Out}}$$  \hfill (4.7)

where

$$A_{v2\text{didt}} = \frac{1}{GK \sqrt{L_1 L_2}}.$$  \hfill (4.8)

Integrating eqn(4.7) with respect to time,

$$I_i = A_{v2\text{didt}} \int V_{didt\text{Out}} dt + C.$$  \hfill (4.9)

The relation between the internal current $I_i$ and the voltage of $s1$, $s2$ is

$$V_{s1} - V_{s2} = R_s (I_i + I_{s2})$$  \hfill (4.10)

and this equation can be converted to

$$V_{s1} - \left(1 + \frac{R_s}{R_t}ight) V_{s2} = R_s I_i$$  \hfill (4.11)

using $I_s = V_i/R_t$, where $R_t$ is the termination resistance 50Ω. From eqn(4.9) and (4.11),

$$V_{s1} - \left(1 + \frac{R_s}{R_t}ight) V_{s2} = R_s A_{v2\text{didt}} \int V_{didt\text{Out}} dt + C.$$  \hfill (4.12)
Differentiate eqn(4.12) by time,
\[ V_{\text{didtOut}} = \frac{1}{R_s A_{2\text{didt}}} \frac{d}{dt} \left[ V_s 1 - (1 + R_s/R_t)V_s 2 \right]. \]  
(4.13)

The detectable \( di/dt \) range and frequency are decided by the amplifier output linearity range and its frequency characteristics
\[ \frac{\text{d} I_i}{\text{d} t} = A_{\text{2didt}} V_{\text{amp \_outRange\_lin}} \]  
(4.14)

and the resolution of the detectable \( di/dt \) is decided by the resolution of the \( di/dt \) detector output voltage
\[ \frac{\text{d} I_i}{\text{d} t} = A_{\text{2didt}} V_{\text{didtOut\_res}}. \]  
(4.15)

### 4.3.2 Design Parameters

The series resistor \( R_s \) on the power supply line is formed using gate-poly with silicide, and the designed resistance value is about 1\( \Omega \). The decoupling capacitor \( C_d \) is formed using poly-poly capacitor, and the designed value is about 700pF. The bias resistor \( R_b \) is formed using gate-poly without silicide and the designed value is about 10\( k\Omega \). The necessary parameter values are listed in Table 4.1.

<table>
<thead>
<tr>
<th></th>
<th>( L_1 )</th>
<th>( L_2 )</th>
<th>( K )</th>
<th>( G )</th>
<th>( A_{\text{2didt}} )</th>
<th>( R_s )</th>
</tr>
</thead>
<tbody>
<tr>
<td>small</td>
<td>0.50nH</td>
<td>14.4nH</td>
<td>0.67</td>
<td>0.39</td>
<td>1.43(nH)(^{-1})</td>
<td>1( \Omega )</td>
</tr>
<tr>
<td>large</td>
<td>0.86nH</td>
<td>53.3nH</td>
<td>0.60</td>
<td>0.39</td>
<td>0.63(nH)(^{-1})</td>
<td>1( \Omega )</td>
</tr>
</tbody>
</table>

### 4.4 Measurement

#### 4.4.1 Setups

The chip was designed and fabricated using 0.35\( \mu \)m 2-Poly 3-ML standard CMOS technology. The chip size is 4.9mm\( \times \)4.9mm and the chip photograph is shown in Fig.4.9.

The chip is mounted on a Cu board as shown in Fig.4.10. The DC bias of \( V_{\text{dd \_i}}, V_{\text{dd \_io}}, V_{\text{dd \_detector}}, V_{\text{ctrl}} \) and \( \text{allORhalf} \) are supplied through lead lines to the islands on the board. The voltage of the islands are stabilized by several chip capacitors. The high-speed output pins including \( \text{didtOut}, \text{CLK/2}, \text{CLK/32}, s1 \) and \( s2 \) are directly probed by 50\( \Omega \) transmission lines so that the signals can be measured by the oscilloscope.
Figure 4.9: Chip photograph. The chip size is 4.9mm×4.9mm.

Figure 4.10: Chip mount on a Cu board.
Since the voltage difference of $s_1$ and $s_2$ is small, attentions should be paid for the precise measurements. The oscilloscope should be calibrated every time when it is turned on. 20dB attenuators are used on the oscilloscope inputs of SIG1, SIG2 and TRIG terminals. Since each attenuator has its own attenuation even though its specification is 20dB, we selected two attenuators which has similar attenuation factor for SIG1 and SIG2 inputs.

### 4.4.2 Sensitivity of the $di/dt$ Detector

Figure 4.11 shows the waveforms of (a) $CLK/2$, (b) $s_1$ and $s_2$, (c) $V_{s_1} - (1 + R_s/R_t)V_{s_2}$ signal and the numerical-time-integral of the $di/dt$ detector output multiplied by $R_sA_{v2didt}$, based on eqn(4.12), (d) the $di/dt$ detector output and the numerical-time-differential of $V_{s_1} - (1 + R_s/R_t)V_{s_2}$ signal divided by $R_sA_{v2didt}$, based on eqn(4.13), of TypeA circuit. The $(M)$ and $(C)$ in the signal caption represent the measured and calculated waveforms, respectively. Since the $V_{s_1} - (1 + R_s/R_t)V_{s_2}$ waveform is noisy, we applied a smoothing before the numerical differentiation.

These graphs show that the currents measured by the series resistor voltage difference and the $di/dt$ detector output have good agreement, and our $di/dt$ detector circuit works well.

### 4.4.3 Accuracy of the $di/dt$ Detector

The series resistance value $R_s$ can be estimated from $s_1$ and $s_2$ voltage difference $\Delta V$ as shown in Fig.4.11(b). Since the internal circuit does not consume current because of no switching at the arrows, the DC current going through the series resistor is the same as the current going into the termination resistor $R_t$ of $s_2$, and $I_{s_2} = V_{s_2}/R_t$. The series resistance value is $R_s = \Delta V/I_{s_2} = R_s\Delta V/V_{s_2} = 50 \times (3.20999 - 3.16070)/3.16070 = 0.78\Omega$. The designed value $R_s=1\Omega$ is a rough estimation, and the measured value $0.78\Omega$ is reasonable.

The current value shown in Fig.4.11(c) vertical axis is calculated using $R_s=0.78\Omega$, and the $di/dt$ value in Fig.4.11(d) vertical axis is calculated using $A_{v2didt}=1.43\times10^9\text{H}^{-1}$. The error between the solid lines and the dashed lines in Fig.4.11(c) and (d) are evaluated by the standard deviation,

$$\sigma = \sqrt{\frac{1}{N - 1} \sum_{i=1}^{N} (V_{solid} - V_{dashed})^2}$$  \hspace{1cm} (4.16)

from 30ns to 65ns region and the number of the sampling points $N$ is about 700. The error in the graph (c) is $\sigma=4.49\text{mV}$ which corresponds to 5.8mA, and the error in the graph (d) is $\sigma=4.38\text{mV}$ which corresponds to $6.3 \times 10^9\text{mA/s}$.
Figure 4.11: Waveforms of (a) CLK/2, (b) s1 and s2, (c) \( V_{s1} - (1 + R_s/R_t)V_{s2} \) signal and the numerical-time-integral of the \( di/dt \) detector output multiplied by \( R_sA_{2didt} \), based on eqn(4.12), (d) the \( di/dt \) detector output and the numerical-time-differential of \( V_{s1} - (1 + R_s/R_t)V_{s2} \) divided by \( R_sA_{2didt} \), based on eqn(4.13), of TypeA circuit. The (M) and (C) in the signal caption represent measured and calculated waveforms, respectively. The current and \( di/dt \) values on the right vertical axis in the graph (c) and (d) are calculated using \( R_s = 0.78 \Omega \) and \( A_{v2didt} = 1.43 \times 10^9 \text{H}^{-1} \), respectively.
4.4.4 Input Impedance of the di/dt Detector

The primary part $L_1$ and $R_1$ of the mutual inductor is inserted in series to the power supply line, and the impedance disturbs the power supply voltage for the internal circuit. Figure 4.12 shows the HSPICE simulation waveform of the voltage drop between the detector terminals $V_1$ using the impedance shown in Fig.4.3 and the current waveform shown in Fig.4.11(c) dashed line.

![HSPICE simulation waveform of the voltage drop between the detector terminals $V_1$](image)

Figure 4.12: HSPICE simulation waveform of the voltage drop between the detector terminals $V_1$ using the impedance shown in Fig.4.3 and the current waveform shown in Fig.4.11(c) dashed line.

Since this is a feasibility experiment, we employ a conservative design for the mutual inductor structure and the peak voltage drop is from $-0.1V$ to $0.2V$. However, the voltage can be reduced with smaller resistance $R_1$ and inductance $L_1$ on the power supply line by using a thicker metal, multi-layer (ML2 and ML3 together, for example), wider power supply line or a straight power supply line with an adjacent spiral inductor if lower sensitivity is acceptable.

4.5 Discussion

4.5.1 Decoupling Capacitor Effects

Figure 4.13 shows the measured waveforms of (a) $s1$, and (b) the $di/dt$ detector output, of TypeA, B, C circuits. The decoupling capacitors of TypeB, C provide AC currents to the internal circuits and the $di/dt$ magnitude in the current through the package parasitic inductance is reduced considerably and hence the power supply voltage bounce are suppressed.
as shown in Fig.4.13(a).

The decoupling capacitor on TypeB circuit suppresses the AC current going through the \( di/dt \) detector so that the \( di/dt \) detector output voltage is small, as shown in Fig.4.13(b). The decoupling capacitor on TypeC circuit provides bigger and sharper AC current to the \( di/dt \) detector compared with the no decoupling capacitor circuit of TypeA. This is because the impedance \( Z_{\text{package}} \) on the power supply line of TypeA works as a current regulator for AC components, while the decoupling capacitor of TypeC works as a constant voltage source.

### 4.5.2 Activation Ratio, Mutual Inductor Dependency

The measured waveforms of \( s1 \) and the \( di/dt \) detector output voltage of TypeA, TypeD, and TypeA of the half activation ratio, are shown in Fig.4.14(a) and (b). The graph (a) shows that the power supply voltage bounce of TypeA and TypeD circuits are almost the same. This is due to the same internal circuits and the same parasitics of the package \( Z_{\text{package}} \), while the \( L_1 \) difference makes the small difference on the waveforms. The half activation case has the half \( di/dt \) of the internal circuit, thus the smaller voltage bounce. The voltage...
Figure 4.14: Measured waveforms of (a) $s_1$, and (b) the $di/dt$ detector output voltage, of TypeA, TypeD, and TypeA of the half activation ratio.

bounce is not a half because of the parasitic capacitance of the internal circuit, the pads, the package and so on.

As for the $di/dt$ detector output waveforms of the Fig.4.14(b), the waveform of TypeD circuit has almost the same shape with about $A_{v2_{di/dt\_large}}/A_{v2_{di/dt\_small}}=2.27$ times magnitude compared with the waveform of TypeA circuit. On the half activation ratio case, the $di/dt$ detector output has about a half magnitude with the same shape.

These results also confirm the $di/dt$ detector performance.

### 4.6 Improved $di/dt$ Detector

#### 4.6.1 Improved Mutual Inductor Structure

As being described in Subsect.4.4.4, the voltage drop by the $di/dt$ detector is too large for a practical use. However, the input impedance and the voltage drop between the terminals of the $di/dt$ detector can be reduced using a straight power line with ML2 and ML3 together as shown in Fig.4.15. The parameters of the improved version of the mutual inductance are
Figure 4.15: Mutual inductance with a lower input impedance.

Table 4.2: Parameters.

<table>
<thead>
<tr>
<th></th>
<th>$L_1$</th>
<th>$R_1$</th>
<th>$K$</th>
<th>$L_2$</th>
<th>$M$</th>
<th>$G$</th>
<th>$A_{v2di/dt}$</th>
<th>$R_s$</th>
</tr>
</thead>
<tbody>
<tr>
<td>small</td>
<td>0.50nH</td>
<td>1.56Ω</td>
<td>0.67</td>
<td>14.4nH</td>
<td>1.80nH</td>
<td>0.39</td>
<td>1.43(nH)$^{-1}$</td>
<td>0.78Ω</td>
</tr>
<tr>
<td>large</td>
<td>0.86nH</td>
<td>2.30Ω</td>
<td>0.60</td>
<td>53.3nH</td>
<td>4.06nH</td>
<td>0.39</td>
<td>0.63(nH)$^{-1}$</td>
<td>0.78Ω</td>
</tr>
<tr>
<td>improved</td>
<td>0.26nH</td>
<td>0.14Ω</td>
<td>0.25</td>
<td>52.3nH</td>
<td>0.92nH</td>
<td>0.76</td>
<td>1.43(nH)$^{-1}$</td>
<td>2.04Ω</td>
</tr>
</tbody>
</table>
listed in Table 4.2. \( L_1 \) becomes half, \( R_1 \) becomes about 1/10 of the small mutual inductor, and the mutual inductance \( M \) becomes half.

In order to measure the waveform in high sensitivity, the gain of the amplifier is designed to be doubled so that the \( A_{v2\text{dt}} \) is almost the same value. Also, \( R_s \) is designed to be larger so that the voltage difference of \( V_{s1} \) and \( V_{s2} \) becomes clear, thus the current measurement for verification purpose becomes easier.

### 4.6.2 Setups

The internal circuit is the same as in Fig.5.5, and its detail will be explained in the next chapter. The overall circuit is the same as in Fig.4.8 except that the internal circuit and the mutual inductor structure are different, and no decoupling capacitor \( C_d \).

The test chip is fabricated as shown in Fig.4.16 using 0.35\( \mu \)m 3-ML 2-poly standard CMOS technology which is the same technology as being used at Fig.4.9. The chip area is 3.0\( \text{mm} \times 1.8\text{mm} \). The test chip is mounted on a Cu board as the same as in Fig.4.10.

![Chip photograph of the improved di/dt detector](image)

Figure 4.16: Chip photograph of the improved di/dt detector. The circuit area is 3.0\( \text{mm} \times 1.8\text{mm} \).

### 4.6.3 Waveforms

The measured waveforms are shown in Fig.4.17. The graphs have the same format as Fig.4.14, and showing the waveforms of (a) \( CLK/2, s1 \) and \( s2 \), (b) \( V_{s1} - (1 + R_s/R_t)V_{s2} \)
Figure 4.17: Waveforms of (a) CLK/2, s1 and s2, (b) \( V_{s1} - (1 + R_s/R_t)V_{s2} \) signal and the numerical-time-integral of the \( di/dt \) detector output multiplied by \( R_sA_{v2didt} \), based on eqn(4.12), (d) the \( di/dt \) detector output and the numerical-time-differential of \( V_{s1} - (1 + R_s/R_t)V_{s2} \) divided by \( R_sA_{v2didt} \), based on eqn(4.13), of the improved \( di/dt \) detector circuit.

The (M) and (C) in the signal caption represent measured and calculated waveforms, respectively. The current and \( di/dt \) values on the right vertical axis in the graph (c) and (d) are calculated using \( R_s=2.04\Omega \) and \( A_{v2didt}=1.43\times10^9H^{-1} \), respectively.
signal and the numerical-time-integral of the $di/dt$ detector output multiplied by $R_sA_{v2didt}$, based on eqn(4.12), (d) the $di/dt$ detector output and the numerical-time-differential of $V_{s1} - (1 + R_s/R_t)V_{s2}$ divided by $R_sA_{v2didt}$, based on eqn(4.13), of the improved $di/dt$ detector circuit. The $(M)$ and $(C)$ in the signal caption represent measured and calculated waveforms, respectively. The current and $di/dt$ values on the right vertical axis in the graph (c) and (d) are calculated using $R_s=2.04\,\Omega$ and $A_{v2didt}=1.43\times10^9\,H^{-1}$, respectively.

The accuracy defined by eqn(4.16) in graph (b) is $\sigma=9.10\,mV$ which corresponds to 4.46mA, and the accuracy in graph (c) is $\sigma=6.30\,mV$ which corresponds to $9.01\times10^9\,mA/s$.

As being listed in Table.4.2, the primary part $L_1$ and $R_1$ of the improved mutual inductor has smaller impedance compared with the conventional small and large mutual inductor. HSPICE simulation waveforms of the voltage drop between the $di/dt$ detector terminals using the impedance listed in Table.4.2 and the current waveform shown in Fig.4.17(b) dashed line are shown in Fig.4.18. The graph shows that the power supply fluctuation caused by the improved $di/dt$ detector is drastically reduced.

![Figure 4.18: HSPICE simulation waveforms of the voltage drop between the detector terminals using the impedance listed in Table.4.2 and the current waveform shown in Fig.4.17(b) dashed line.](image)

Sect.4.6. Improved $di/dt$ Detector  75
4.7 Feedback di/dt Control

4.7.1 Implementation

The di/dt detector can be used for an automatic di/dt control system since the detector is realized on-chip and outputs the di/dt value in real time without any numerical calculation. For example, the di/dt value is always under observation by the di/dt detector and controls the activation ratio of the internal circuit in accordance with the di/dt value.

Figure 4.19 shows an example of the feedback di/dt control system. The di/dt detector outputs the di/dt value, and the Gilbert multiplier[19] multiplies the value and converts into di/dt power waveform. Then the low pass filter outputs the di/dt proportional DC voltage. The comparators compare the DC voltage with reference voltages. When the di/dt exceed a threshold VrefH, Overflow signal gets “H” and the sleep controller outputs “L (sleep)” to the activeORsleep node so that the half of the internal circuit is turned off and the di/dt is reduced, resulting Overflow signal becomes “L”. If the di/dt still exceed a threshold even though the half of the circuit is turned off, the Overflow signal always outputs “H”. When di/dt is reduced to below the threshold VrefL, the sleep controller outputs “H (active)” so that all the internal circuit is turned on.

The schematic of the Gilbert multiplier, whose analog output voltage is proportional to \((V_{in1} - V_{in2}) \times (V_{in3} - V_{in4})\), is shown in Fig.4.20. Here, \(in1 - in3\) and \(in2 - in4\) are connected so that the output voltage is proportional to the di/dt power. The schematic of the sleep controller is shown in Fig.4.21.

The test circuit is designed using 0.15\(\mu\)m 5-ML 1-Poly SOI-CMOS technology, and the circuit area is 2.5mm\(\times\)1.3mm as shown in Fig.4.22.

![Feedback di/dt control system](image_url)
Figure 4.20: Gilbert multiplier.

Figure 4.21: Sleep control.
4.7.2 Simulation Waveforms

HSPICE simulation waveforms are shown in Fig.4.23. The power supply voltage is swept from 0.5V to 1.5V so that the power consumption and $\frac{di}{dt}$ of the internal circuit are increased. All the internal circuit is active at time (i) until $LPout$ exceeds $V_{refH}$ at time (ii). Then, the sleep signal is ON and the half of the internal circuit is OFF so that the $\frac{di}{dt}$ is reduced. The $\frac{di}{dt}$ exceeds the reference value even though half of the internal circuit is sleeping at time (iii), and the $Overflow$ signal is ON. As lowering the power supply, $\frac{di}{dt}$ is reduced below $V_{refH}$ and the $Overflow$ is OFF at time (iv). At time (v), the $\frac{di}{dt}$ is reduced below $V_{refL}$ and then the active signal is ON so that all the circuit start to operate.

The waveforms show that the feedback $\frac{di}{dt}$ control circuit works as being designed.

4.8 Summary

The on-chip $\frac{di}{dt}$ detector has been demonstrated. Our $\frac{di}{dt}$ detector consists of a power supply line, an underlying spiral inductor and an amplifier. The mutual inductor induces a $\frac{di}{dt}$ proportional voltage, and the amplifier amplifies and outputs the value. The measurement results show that the $\frac{di}{dt}$ detector output and the voltage difference between resistor terminals have good agreement with the accuracy of $6.3 \times 10^9$ mA/s. The current waveform can be obtained with the accuracy of 5.8mA by integrating the $\frac{di}{dt}$ waveform. The $\frac{di}{dt}$ detector also detects decoupling capacitor effects for $\frac{di}{dt}$ reduction.

An improved version of the $\frac{di}{dt}$ detector circuit is also implemented. A straight power
Figure 4.23: HSPICE simulation waveforms of the feedback \( di/dt \) control circuit.
supply line by ML2 and ML3 together reduces the input impedance of the primary part, and the voltage drop of the $di/dt$ detector is drastically suppressed. Measurement results shows that the improved $di/dt$ detector has similar sensitivity and accuracy compared with the original one.

Since on-chip and real-time $di/dt$ measurements are possible, our $di/dt$ detector circuit can be applicable for feedback $di/dt$ control as well. Simulation results show that the feedback $di/dt$ control circuit using the $di/dt$ detector turns off the half of the internal circuit when the $di/dt$ exceeds a threshold, and turns on the slept circuit again when the $di/dt$ value goes down below a threshold.
Chapter 5

Feedforward Active Substrate Noise Cancelling Technique using Power Supply di/dt Detector

Abstract

This chapter demonstrates a feedforward active substrate noise cancelling technique using a power supply di/dt detector. Since the substrate is tied to the ground line, the substrate noise is closely related to the ground bounce which is caused by di/dt when inductance is dominant on the ground line impedance. Our active cancelling technique detects the di/dt of the power supply current and injects an anti-phase signal into the substrate so that the di/dt proportional substrate noise is cancelled out. 34% of the substrate noise reduction was achieved in a test circuit. It is theoretically shown that the optimized canceller design will enhance the suppression ratio up to 56%.
5.1 Introduction

As the growing demand of analog-digital mixed signal LSIs such as A/D, D/A and PLL integrated with large scale digital circuits, substrate noise becomes serious concern. Although power lines for digital and analog circuits are isolated in order to prevent the coupling of the digital switching noise to the analog circuits, the digital switching noise is transferred to the analog blocks via the common substrate. It was reported that a PLL jitter is 10 times degraded by substrate noise[20].

In digital CMOS circuits, the substrate noise is caused by three mechanisms: coupling from the digital power supply, coupling from switching of source/drain nodes, and impact ionization in MOSFET channels[21]. Noise on a power line is caused by $di/dt$ noise and resistive voltage drops due to the parasitic impedance of the power line. Typically, the digital ground line is connected to the substrate in every CMOS gate, which results in a very low resistance between the digital ground line and the substrate, and hence the digital ground noise and ringing will also be present on the substrate. This noise coupling mechanism is often the dominant cause of substrate noise. One report shows that the substrate noise has the same shape with 1/8 amplitude of the ground noise[16].

Guard rings are widely used to suppress the substrate noise. However, the parasitic impedance of the guard line degrades the efficiency of the noise absorption especially for high frequency noise[22]. Another method is a feedback active guard band filtering[22][23]. The anti-phase noise signal is actively supplied to the guard band so that the original substrate noise is cancelled out. In this technique, an amplifier is used to sense the original substrate noise and generates the anti-phase noise signal. However, the frequency response and the delay of the amplifier restricts the bandwidth of the cancellable noise, so that the noise reduction ratio is not enough for practical applications. And feedback systems are sometimes unstable.

This chapter demonstrates a feedforward active substrate noise cancelling technique using a $di/dt$ detector.

In Sect.5.2, the circuit design for the feedforward active noise cancelling is described. Section 5.3 shows measurement results. Discussions will be given in Sect.5.4, and Sect.5.5 summarizes this chapter.
5.2 Circuit Design for Feedforward Active Substrate Noise Cancelling

5.2.1 Substrate Noise and di/dt

The main cause of substrate noise is a coupling from digital power lines. Ground noise is caused by the supply current and the ground line impedance. The ground noise amplitude is proportional to the \( di/dt \) if inductance is dominant in the ground line impedance. Therefore, the substrate noise is also proportional to the \( di/dt \). Here, the \( di/dt \) detector described in the previous chapter can be applicable for cancelling the \( di/dt \) proportional substrate noise.

A block diagram of our feedforward active substrate noise cancelling system is shown in Fig.5.1. The ground noise is caused by the power supply \( di/dt \) and \( L_{gnd} \). The ground noise is transferred to the analog circuit through the substrate resistance. The p-sub/Nwell junction capacitor is negligibly small compared with the ground line-substrate impedance that the \( Vdd_D \) bounce is not transferred to the substrate. Since the substrate noise is proportional to the \( di/dt \), the \( di/dt \) detector inverted output has anti-phase against the substrate noise. If the anti-phase signal is injected into the substrate, it can cancel the original substrate noise.

![Figure 5.1: Feedforward active substrate noise cancelling.](image-url)
5.2.2 Noise Canceller

The substrate noise canceller is basically the same as the \( \frac{di}{dt} \) detector described in the previous chapter, where a mutual inductor coupled to the power supply line induces the \( \frac{di}{dt} \) proportional voltage, and an amplifier amplifies and outputs the value. The difference of the noise canceller is that the plus-minus terminals of the amplifier inputs from the mutual inductor are exchanged in order to generate the “anti”-phase signal, as shown in Fig.5.2.

Since the substrate is tied to the ground voltage, the coupling capacitor \( C_c \) is inserted at the output of the amplifier to prevent the bias voltage change of the node \( n2 \). Here, the input impedance of the substrate from the injection point is assumed to be pure resistive. In order to inject the current with the appropriate phase, the impedance of the coupling capacitor \( C_c \) should be small enough compared with the substrate resistor impedance. Then, the amplifier can be considered as a voltage controlled current source. Therefore, the injected current has the same phase as \(-V2\) which has the anti-phase against the \( \frac{di}{dt} \).

![Figure 5.2: Active substrate noise canceller.](image)

5.2.3 Substrate Noise Probing for Verification

The substrate noise probing circuit implemented for verification purpose is shown in Fig.5.3. The noise is probed using an differential amplifier at the first stage with one input connected to the substrate and the other to an external ground as a reference. The input terminals are biased as half-Vdd by the resistors \( R_b \), where the amplifier has the maximum gain. The resistance is large enough to be considered as open for AC signals. Since the substrate voltage is around ground voltage, the coupling capacitors \( C_c \) are used here as...
The second and the third stage amplifiers are composed of PMOS and resistors, and the final stage is a PMOS open drain structure.

Since substrate contacts of NMOS may change the substrate noise waveform, the body terminals of MN1 in the amplifier are not tied even though it may lead to an unstable amplifier operation. The second and third stage amplifiers are composed without NMOS to eliminate the substrate contacts. Here, the ratio of $\Delta I_d/\Delta V_g$ and $\Delta I_d/\Delta V_{bs}$, which is $g_m/g_{bs}$, is 6.0 as shown in Fig. 5.4 according to HSPICE simulation. Thus, the amplifier has enough gain even though the noise voltage for the gate and the substrate are the same.

![Figure 5.3: Substrate noise prober.](image)

![Figure 5.4: Ratio of $g_m$ and $g_{bs}$.](image)
5.2.4 Internal Circuit as Noise Source

Figure 5.5 shows our internal circuit as a noise generator. The test circuit contains VCO so that we can easily sweep the operating frequency by changing the DC control voltage ($V_{ctrl}$). The frequency divider generates 101010… signal for the input to the shift register. The SEL circuit can select the operating mode, a repeat mode or a random mode. On the repeat mode, the SEL circuit always outputs “High” signal, the signal change from the DFFs are transferred to the inverter chains and the circuit consumes the same amount of current at every clock cycle. On the random mode, the SEL circuit passes $CLK/4$, $CLK/8$ signals, the DFF outputs and some inverter chains are disconnected when the SEL outputs are “Low”, and hence the current waveform becomes different in accordance with the divided clock signals. $allORhalf$ signal controls the activation ratio of the circuit. The $CLK/32$ output is used as a trigger for a oscilloscope, and the $CLK/2$ output is used as a reference for the timing consideration.

Figure 5.5: Internal circuit as a noise source.
5.2.5 Design Parameters

The circuit is designed using 0.35\(\mu\)m 3-ML 2-Poly standard CMOS technology. The mutual inductor of the \(\frac{di}{dt}\) detector consists of the power supply line and an underlying spiral inductor. The power supply line \(L_1\) is composed of the top metal layer ML3 with 1 turn, 20\(\mu\)m width. The spiral inductor \(L_2\) has 24 turns with 2\(\mu\)m width and 2\(\mu\)m spacing using ML1. The outside diameter of the both inductors are 200\(\mu\)m \(\times\) 200\(\mu\)m. The equivalent circuit of this mutual inductor structure is extracted by FastHenry[11] 3D field solver. The coupling capacitor \(C_c\) is formed using poly-poly capacitor, and the designed value is about 25pF. The bias resistor \(R_b\) is formed using gate-poly without silicide and the designed value is about 10k\(\Omega\). The necessary parameter values are listed in Table 5.1.

<table>
<thead>
<tr>
<th>mutual inductor</th>
<th>(L_1)</th>
<th>(L_2)</th>
<th>(K)</th>
<th>(R_1)</th>
<th>(R_2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.86nH</td>
<td>53.3nH</td>
<td>0.603</td>
<td>2.3(\Omega)</td>
<td>218(\Omega)</td>
</tr>
<tr>
<td>amp for canceller</td>
<td>(W_{pmos})</td>
<td>(W_{nmos})</td>
<td>(R_b)</td>
<td>(C_c)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>200(\mu)m</td>
<td>100(\mu)m</td>
<td>10k(\Omega)</td>
<td>25pF</td>
<td></td>
</tr>
<tr>
<td>amp for prober</td>
<td>(W_{pmos1})</td>
<td>(W_{nmos1})</td>
<td>(R_b)</td>
<td>(C_c)</td>
<td>(W_{pmos2})</td>
</tr>
<tr>
<td></td>
<td>20(\mu)m</td>
<td>10(\mu)m</td>
<td>10k(\Omega)</td>
<td>25pF</td>
<td>160(\mu)m</td>
</tr>
</tbody>
</table>

5.2.6 Floorplan

Figure 5.6 shows a chip photograph of our test circuit. The chip area is 3.0mm \(\times\) 1.8mm.

The substrate noise probing point is located 750\(\mu\)m apart from the noise source, and the cancel signal injection area is located between the noise source and the probing point.

5.3 Measurement

5.3.1 Setups

In order to measure high-speed noise waveforms, the chip is mounted on a Cu board as shown in Fig.5.7. All the inputs including \(Vdd\)\_internal, \(Vdd\)\_io, \(Vdd\)\_canceller, \(Vdd\)\_prober, \(Vctrl\), \(SEL\) and \(allORhalf\) are DC and supplied through lead lines to the “islands” on the board. The voltage of the islands are stabilized by several chip capacitors. 50\(\Omega\) transmission lines are directly connected to the high-speed output pins including \(CLK/2\), \(CLK/32\) and the substrate noise prober output, in order to reduce reflections.
Figure 5.6: Chip photograph of the feedforward active substrate noise cancelling circuit, fabricated by 0.35µm standard CMOS technology. The chip area is 3.0mm×1.8mm.

Figure 5.7: Photograph of the chip mount.
5.3.2 Substrate Noise Waveforms

The measured waveforms of the substrate noise and the $CLK/2$ signals are shown in Fig.5.8. The active cancel OFF/ON means $V_{dd\text{-canceller}}=0V/3.3V$. Figure 5.8(a) is on the

![Waveform Diagram](image)

Figure 5.8: Substrate noise waveforms with the active noise cancelling ON/OFF, together with the $CLK/2$ signal. The operating frequency is 500MHz. (a) Repeat mode, and (b) Random mode.
repeat mode, and Fig.5.8(b) is on the random mode. The operating frequency is 500MHz, and the gain of the noise prober at this frequency is about 7.5 by HSPICE simulation. The prober output has about 1V bias because the on-resistance of the final stage PMOS of the prober circuit is about 100Ω, as shown in Fig.5.3. The graphs show that our feedforward active cancelling circuit cancels and reduces the substrate noise of 30% on the repeat mode and 24% on the random mode if the peak-to-peak voltages are concerned.

5.3.3 Frequency Dependence

The frequency dependence of the upper and lower peaks of the substrate noise voltage, together with its suppression ratio, on the repeat mode are shown in Fig.5.9(a) and on the random mode in Fig.5.9(b). 17% to 34% of the substrate noise is suppressed from 100MHz to 600MHz operation range on the repeat mode, and 15% to 31% of the noise is suppressed on the random mode, by our feedforward active substrate noise cancelling circuit. The noise suppression ratio does not degrade over 600MHz operation on the random mode because the dominant noise component becomes the half of the operating frequency because of the random mode operation.

5.4 Discussion

5.4.1 Current Injection

The amplitude of the injected current for the noise cancelling is controlled by the noise canceller supply voltage $V_{dd\_canceller}$, and $V_{dd\_canceller}$ dependence of the substrate noise is shown in Fig.5.10. The graph shows the upper and lower peak voltage change at 500MHz operation on the repeat mode. It is shown that the substrate noise starts to be reduced around 1.0V as the cancelling signal increases until being saturated around 2.5V. It is because the noise injection amplifier starts to operate over 1.0V, and its gain is saturated around 2.5V because the transconductance $g_m$ of MP1 and MN1 saturates.

The phase and amplitude of the substrate noise is plotted in a phasor diagram as shown in Fig.5.11. The phase is relative to $CLK/2$. The trace of the phasor with $V_{dd\_canceller}$ sweeping from 0V to 3.3V by 0.1V step shows that the phase of the injected current in this graph is $-\pi/2$. It also shows that more current injection by using bigger transistor width for MP1 and MN1 of the canceller amplifier will suppress more substrate noise. The minimum substrate noise by using the optimum MP1 and MN1 is $V_{min}$ in Fig.5.11, and the optimum noise suppression ratio is 56%. $V_{min}$ depends on the phase difference between the substrate...
Figure 5.9: The frequency dependence of the upper and lower peaks of the substrate noise voltage, together with its suppression ratio by the feedforward active noise cancelling (a) on the repeat mode, (b) on the random mode.
Figure 5.10: Noise canceller supply voltage dependence of the substrate noise amplitude, on the repeat mode at 500MHz operation with the anti-phase current injection.

Figure 5.11: Noise canceller supply voltage dependence of the substrate noise phasor, for $V_{dd\_canceller}$ sweeping from 0V to 3.3V by 0.1V step, on the repeat mode at 500MHz operation with the anti-phase current injection.
noise and the $di/dt$. If the phase of the substrate noise and $di/dt$ completely match (i.e. $\theta=0$), $V_{\text{min}}$ could be zero.

The anti-phase current is injected to cancel the substrate noise here. Another type of injection circuit, whose plus-minus terminals of the amplifier inputs are exchanged to realize “in”-phase current injection, has been implemented for a reference. Other circuits are exactly the same and the chip photograph looks the same as Fig.5.6. The in-phase current injection increases the substrate noise as shown in Fig.5.12. It supports the model that the substrate noise reduction in the previous section is realized by our feedforward active cancelling scheme, not by other reasons. The cause of the substrate noise difference between the anti-phase and the in-phase at $V_{\text{dd_canceller}}=0$ in Fig.5.10 and Fig.5.12 is considered as the process variation. Since the test chips of the anti-phase injection and the in-phase injection are different, the offsets and gains of the noise canceller and the noise prober have different characteristics in each chip.

![Figure 5.12](image)

Figure 5.12: Noise canceller supply voltage dependence of the substrate noise amplitude, on the repeat mode at 500MHz operation with the in-phase current injection.
5.5 Summary

A feedforward active substrate noise cancelling scheme has been demonstrated. Our active cancelling technique detects the $\frac{di}{dt}$ of the power supply current and injects an anti-phase signal into the substrate so that the $\frac{di}{dt}$ proportional substrate noise is cancelled out. 30% of the substrate noise reduction was achieved in our 500MHz operating test circuit, and 17% to 34% of the substrate noise reduction is observed from 100MHz to 600MHz range. The substrate noise phasor measurement result shows that the optimum transistor width of the current injection amplifier will enhance the noise suppression ratio up to 56%.
Chapter 6

Conclusions

Power Line Noise Reduction in LSI was discussed in this dissertation. Conclusions in our activities are as follows:

**Chapter 2.** Stubs and decoupling capacitors are compared for power supply noise reduction points of view. Stubs have been widely used for impedance matching techniques, and the input impedance of a quarter-length stub is close to zero for a specified frequency. The power line noise can be reduced by attaching the quarter-length stub to the power line of an LSI.

The input impedance of a stub and a capacitor with the same area $A$ is formulated using the thickness $t$, the distance $d$, the resistivity $\rho$ and the relative dielectric constant $\epsilon_r$. Then, the boundary frequency $f_B$ above which the stub input impedance is lower than the capacitor impedance is clarified. The analytical models show that the stub works more efficiently as the noise frequency gets higher. The analytical models are confirmed by numerical analysis conducted by field solvers.

Circuit simulation results show that the stub reduces 37% and 18% of the power supply noise compared with the nothing attached case and the decoupling capacitor case, respectively, in a 1.8V 2.5GHz test circuit with $d = 5\mu m$, $t = 1\mu m$, $A=1mm^2$, $\epsilon_r=3.9$, $\rho = 1.673 \times 10^{-8}\Omega\cdot m$ case.

**Chapter 3.** Power supply noise reduction effects of stubs are experimentally demonstrated. An on-chip stub on a 2.5GHz operation LSI does not shows its noise reduction mainly because of the parasitic resistance and reflections occurring at the bendings along its length as long as over 15mm. On-board stubs and off-chip stub, on the other hand, clearly reduce the power supply noise as theoretically predicted in Chap.2.
The measurement results show that the on-board stubs for 1.25GHz, 1.95GHz remove 87%, 72% of the designed frequency noise and 39%, 19% of the total noise of our test circuit, and 90% of the designed frequency noise component and 48% of the total noise are reduced when the off-chip stubs are attached to the 1.15GHz operating test chip, respectively. It is also observed that the noise other than the stub-designed frequency is not suppressed, showing the band-eliminate characteristics of the stubs, as being theoretically predicted in Chap.2.

The measurement results also indicate the possibility of stub on-chip integration which can eliminate package and bonding wire impedance effects for the internal circuit, when a LSI operating frequency becomes higher and the stub length becomes shorter.

Chapter 4. An on-chip $\frac{d}{dt}$ detector are demonstrated. The on-chip $\frac{d}{dt}$ detector consists of a power supply line, an underlying spiral inductor and an amplifier. The mutual inductor induces a $\frac{d}{dt}$ proportional voltage, and the amplifier amplifies and outputs the value. The diameter of the mutual inductor structure is 140µm. The amplifier is designed to have small gain, 0.39, with 50Ω termination resistance so as to have a high cut-off frequency, which is 2.2GHz.

The voltage difference of the resistor terminals inserted in series to the power supply line shows its current waveform, and the $\frac{d}{dt}$ can be obtained by differentiate the current waveform by time. Also, the current waveform can be obtained by integrating the $\frac{d}{dt}$ detector output waveform.

Measurement results show that the $\frac{d}{dt}$ detector output and voltage difference between the resistor terminals have good agreement with the accuracy of $6.3 \times 10^9$ mA/s for the $\frac{d}{dt}$, and with the accuracy of 5.8mA for the current waveforms. The $\frac{d}{dt}$ detector also detects the decoupling capacitor effects for the $\frac{d}{dt}$ reduction.

An improved version of $\frac{d}{dt}$ detector is also implemented. The power supply line, which is a primary part of the mutual inductor, has just a straight layout consisting of ML2 and ML3 together instead of one turn spiral with ML3, so that the voltage drop between the $\frac{d}{dt}$ detector is drastically reduced. Measurement results show that the improved $\frac{d}{dt}$ detector has similar sensitivity and accuracy compared with the original one.

One of the applications of the $\frac{d}{dt}$ detector is a feedback $\frac{d}{dt}$ controller. The $\frac{d}{dt}$ detector output is multiplied and filtered by a low pass filter such that the $\frac{d}{dt}$ power is converted into a DC voltage. The $\frac{d}{dt}$ controller can output a sleep signal for the
internal circuit when the \( di/dt \) proportional voltage exceeds a threshold. Simulation results show that the feedback \( di/dt \) controller works as being designed.

**Chapter 5.** A feedforward active substrate noise cancelling scheme is demonstrated. Since the substrate is tied to the ground line, the substrate noise is closely related to the ground bounce which is caused by \( di/dt \) when inductance is dominant on the ground line impedance. The feedforward active cancelling technique detects the \( di/dt \) of the power supply using the \( di/dt \) detector described in Chap.4, and injects the anti-phase signal into the substrate so that the \( di/dt \) proportional substrate noise is cancelled out.

A substrate noise prober for verification purpose is proposed as well. In order not to disturb the original substrate noise waveforms, p-substrate-contact-free amplifier is developed.

Measurement results show that 30\% of the substrate noise reduction was achieved in our 500MHz operating test circuit, and 17\% to 34\% of the substrate noise reduction is observed from 100MHz to 600MHz range. The substrate noise phasor measurement result shows that the optimum transistor width of the current injection amplifier will enhance the noise suppression ratio up to 56\%.

Now we are sure that these results in this dissertation such as power supply noise reduction using stubs, the on-chip \( di/dt \) detector, and the feedforward active substrate noise cancelling using the \( di/dt \) detector will make a large contribution to improve the signal integrity issues and also future LSI developments.
Bibliography


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List of Presentations and Publications

- **Publications**

- **Presentations**

– 名倉 徹, 大池 祐輔, 池田 誠, 浅田 邦博 “オフチップスタブを用いた LSI における電源ノイズ低減,” 電子情報通信学会ソサイエティ大会, C-12-1, pp.71, 2004年9月 (Chapter 3)