A Study on Power Line Noise Reduction in Large Scale Integration 半導体集積回路における電源ノイズ低減に関する研究 Toru Nakura

Supervisor: Prof. Kunihiro Asada

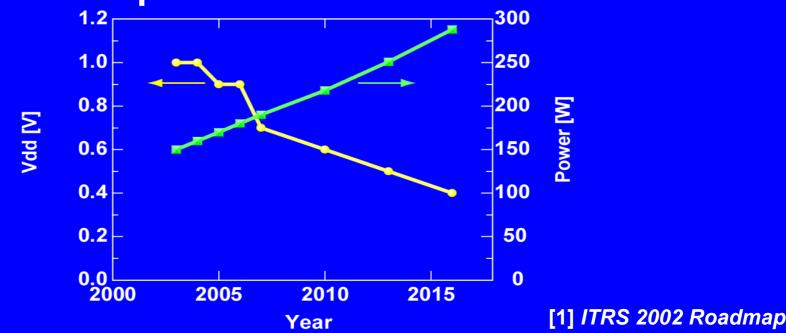
Dept. of Electronic Engineering, University of Tokyo, Tokyo, Japan

Jan. 27, 2005

Final Defense for Ph.D

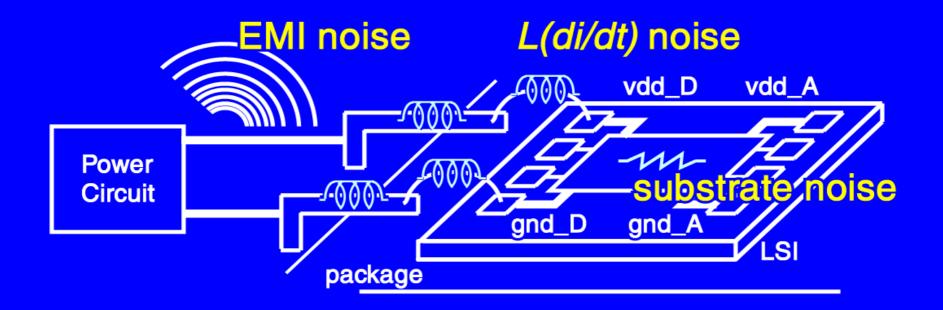
#### Introduction

- Power supply voltage will decrease
   Noise margin will be reduced
- Power and currents will increase
   Noise amplitude will be increased



# Signal Integrity and di/dt

- Power supply noise : L(di/dt)
- EMI noise : caused by di/dt
- Substrate noise : related to power noise



# **Signal Integrity Problems**

- Power supply noise
  - Timing violation delay  $\propto 1/(Vdd-Vth)$
  - Logic error
- Substrate noise
  - PLL jitter becomes 10 times bigger by the substrate noise [20]
- EMI noise
  - Operational problems in other devices
  - Regulations has been enforced [2]

[20] *P. Larsson, JSSC July 2001* [2] *VCCI* 

# **Improve Signal Integrity**

- Reduce the di/dt
- Measure the di/dt
- Use the di/dt for substrate noise reduction

## Contents

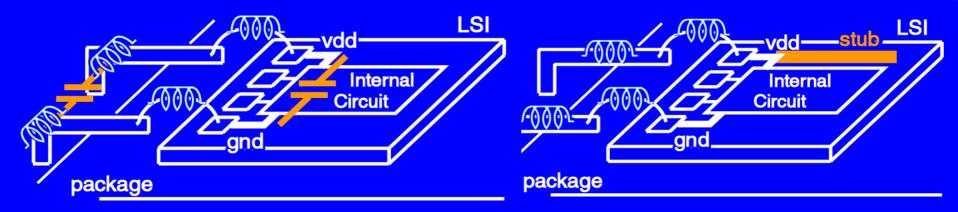
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- Comparison of stubs and decoupling capacitor for noise reduction
- Experiments for power supply noise reduction using stubs
- On-chip di/dt detector for power supply
- Feedforward active substrate noise cancelling using the di/dt detector
- Conclusions

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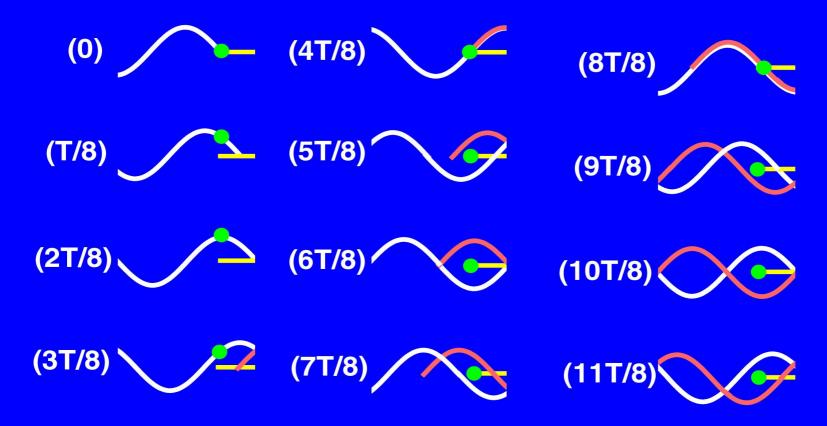
## **Background – di/dt Reduction –**

- Decoupling capacitor
  - Area penalty, parasitic inductance
- Attach the stub to the power line will reduce the power supply noise

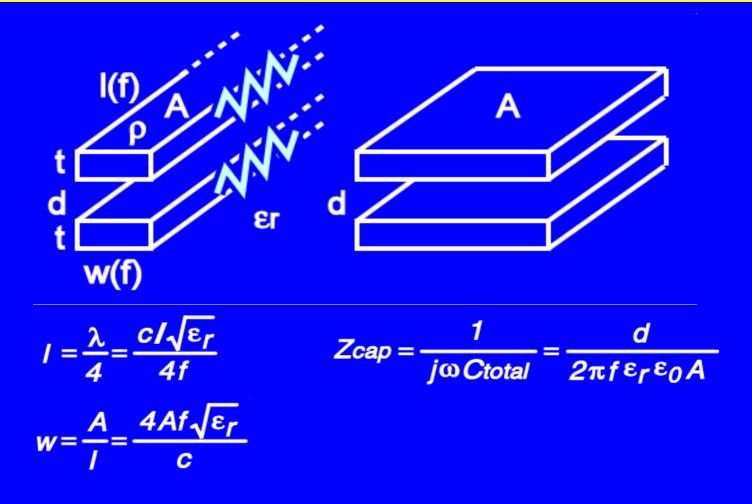


## Waveform in Ideal λ/4 Stub

 The forward- and backward-going waves are cancelled



## **Stub and Capacitor Impedance**



Zstub = ...

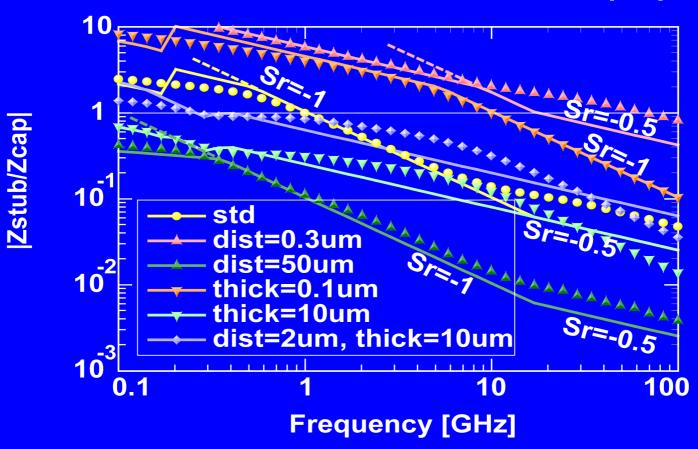
## **Boundary Frequency**

- Stub input impedance Zstub ∝f<sup>-2</sup>, f<sup>-1.5</sup>
- Capacitor input impedance Zcap ∝f<sup>-1</sup>
- Boundary frequency at Zstub=Zcap

$$fB = \frac{\pi c^2 \varepsilon_0 \rho}{8td} \qquad \frac{t^3}{A} < \frac{16\rho\sqrt{\varepsilon_r} \varepsilon_0 c}{\pi} \quad \text{and} \quad t < \frac{16d}{\pi^2}$$
$$\frac{t^3}{A} > \frac{16\rho\sqrt{\varepsilon_r} \varepsilon_0 c}{\pi} \quad \text{and} \quad t > \frac{\pi^3 c \sqrt{\varepsilon_r} \varepsilon_0 \rho A}{64d^2}$$
$$fB = \frac{\pi^3 c^2 \varepsilon_0 \rho}{256d^2} \qquad \frac{t^3}{A} < \frac{16\rho\sqrt{\varepsilon_r} \varepsilon_0 c}{\pi} \quad \text{and} \quad t > \frac{16d}{\pi^2}$$
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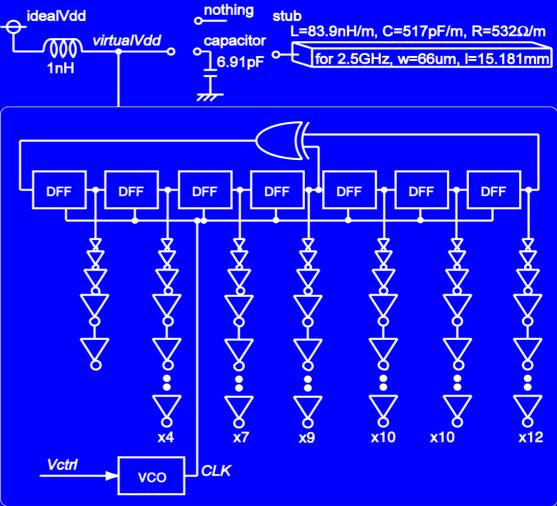
## **Numerical Analysis**

- Raphael(L,C), Fasthenry(R) vs. the model
- d=5um, t=1um, A=1mm<sup>2</sup>, εr=3.9, ρ=ρCu

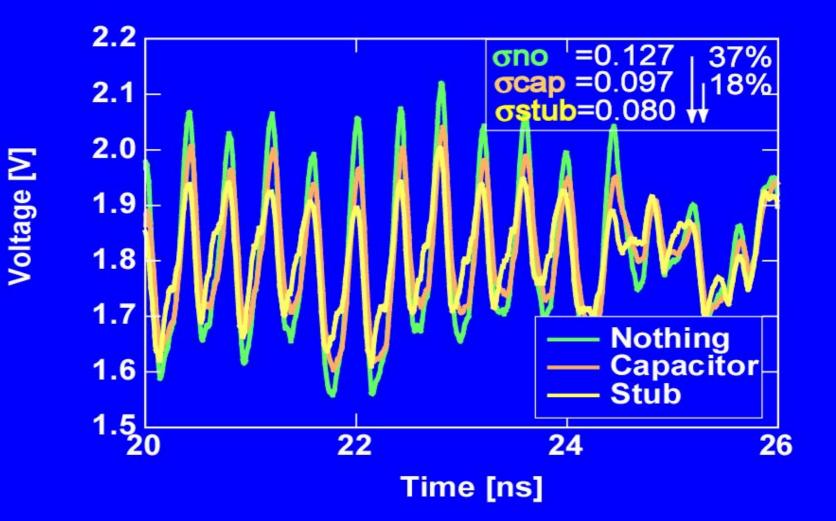


## **Circuit Simulation**

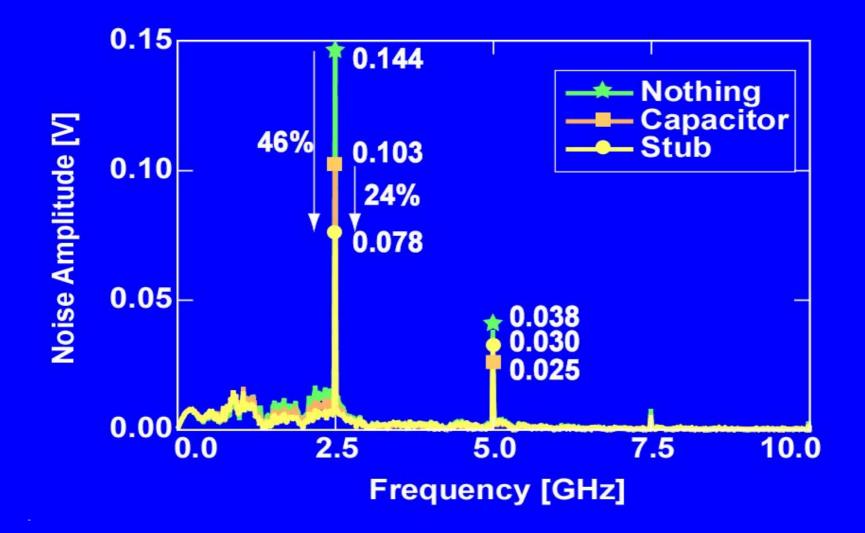
- 0.18um CMOS \_\_\_\_idealVdd
- *fop*=2.5GHz



# **Power Supply Noise Waveform**



# **Power Supply Noise Spectrum**



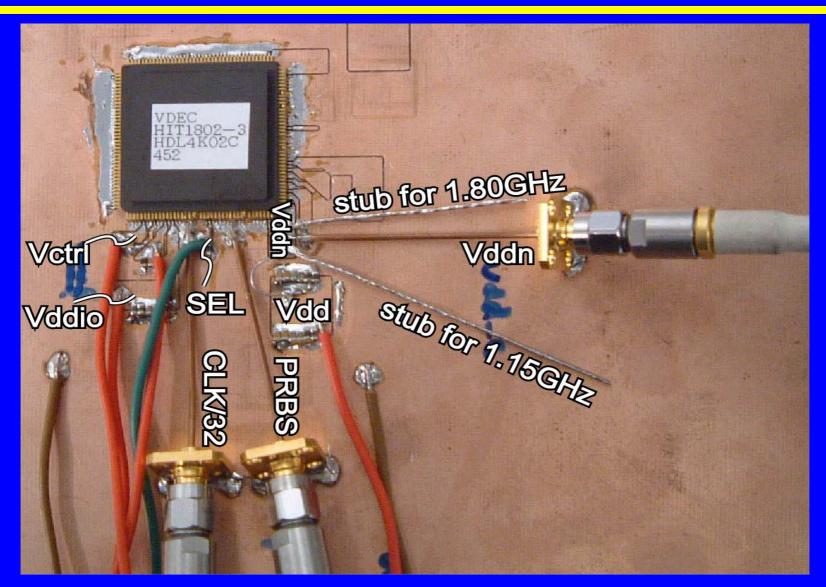
# **Short Summary**

- Stubs and capacitors are compared for power supply noise reduction
- Boundary frequency above which stubs are more effective than decoupling capacitors is clarified
- Circuit simulation shows that the stub reduces 37% and 18% of the power supply noise compared with the nothing and the capacitor case.
- It is theoretically shown that stubs will have more advantage over capacitors for LSIs with higher operating frequency

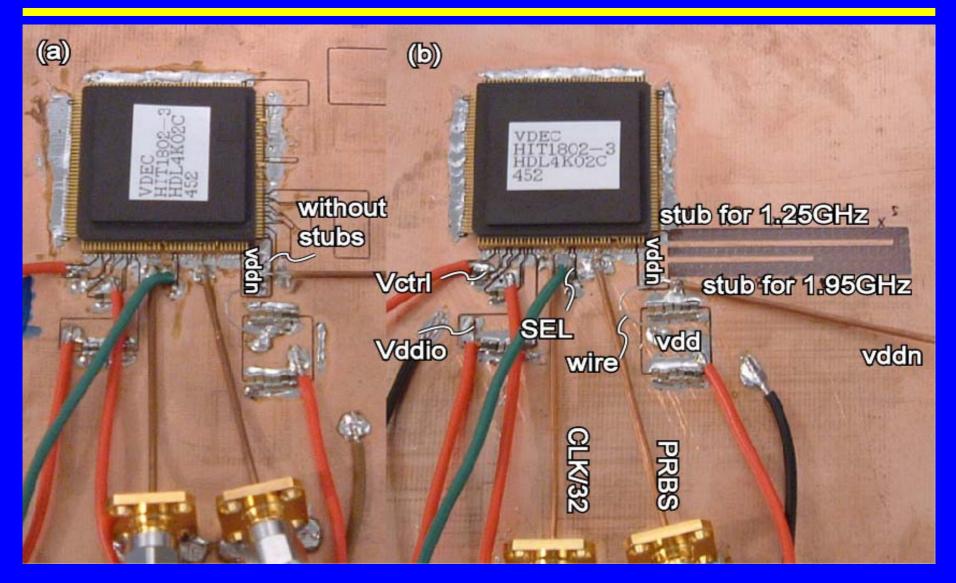
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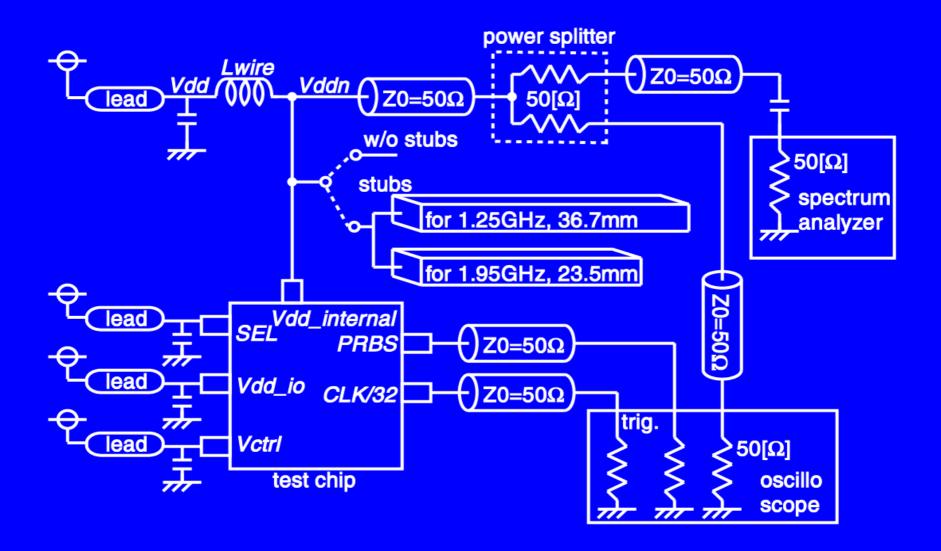
## **Off-chip Stubs**



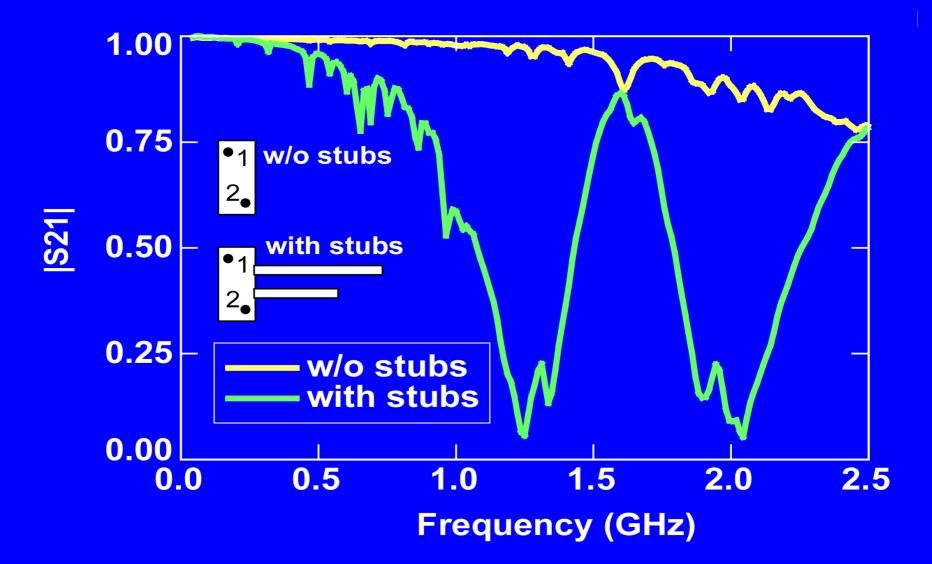
## **On-board Stubs**



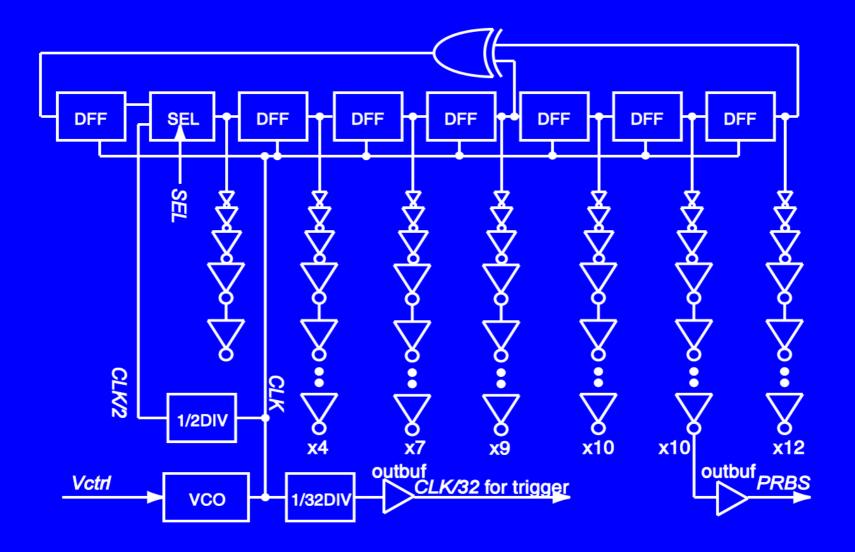
## **Schematic**



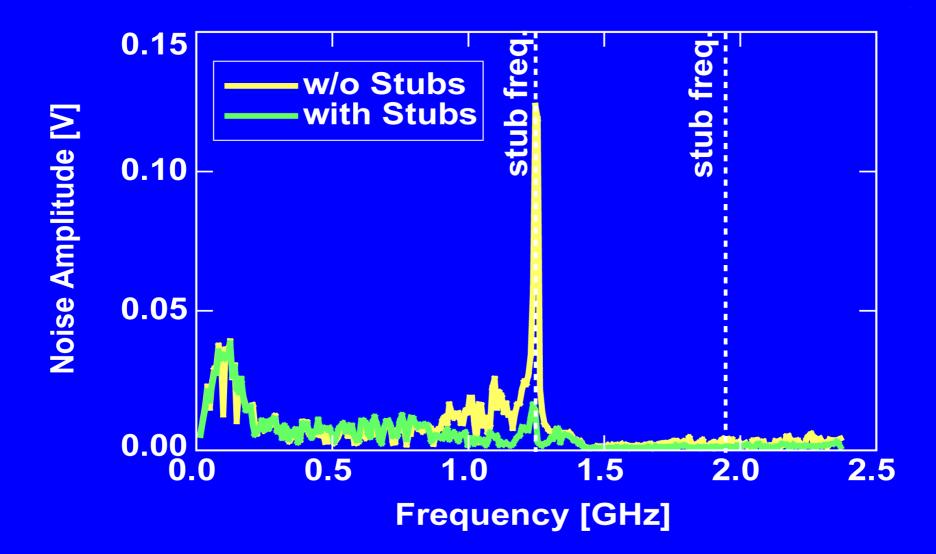
# S parameter – S21



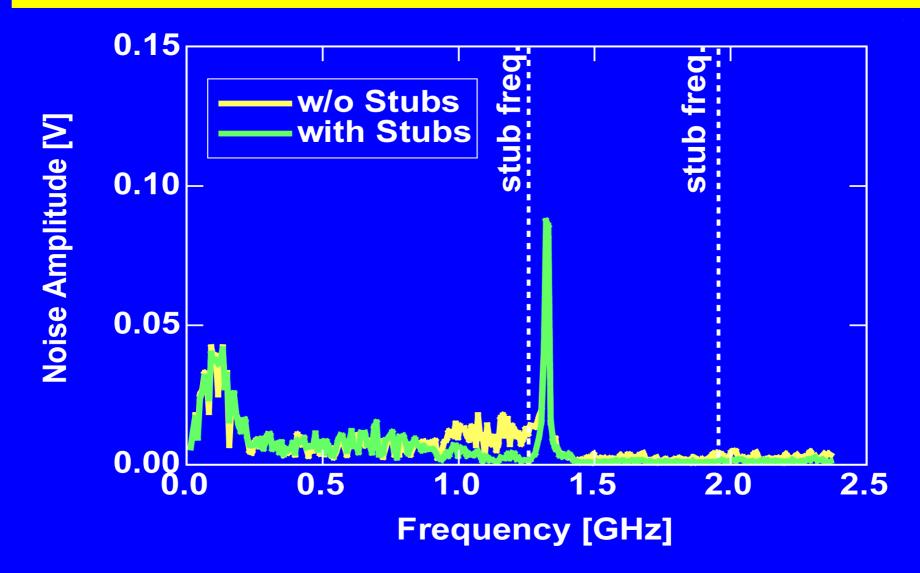
## **Internal Circuit**



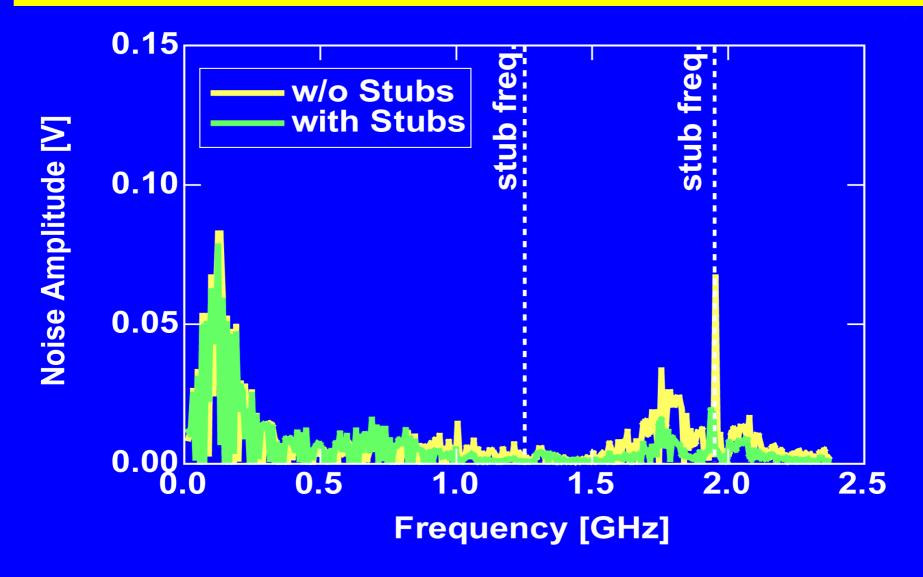
# Freq. Dependence @1.25GHz



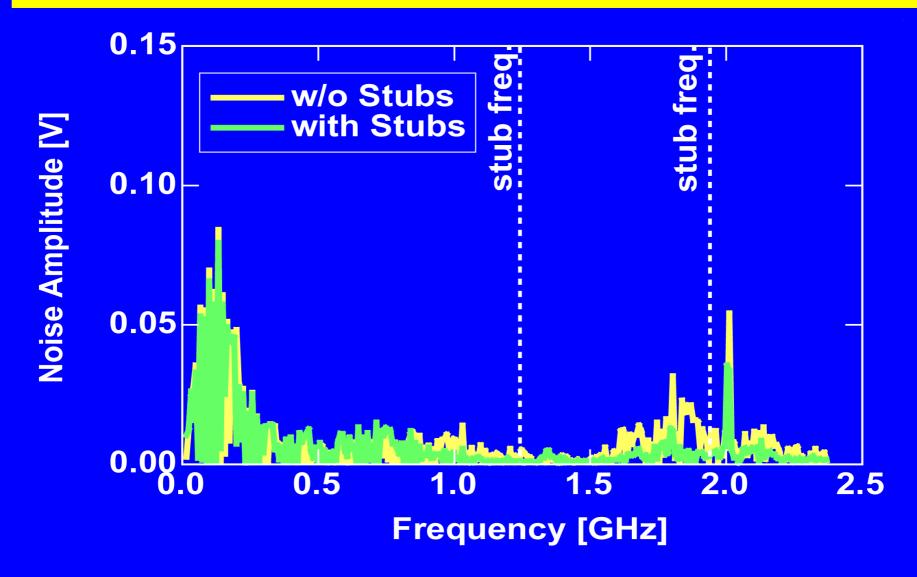
# Freq. Dependence @1.32GHz



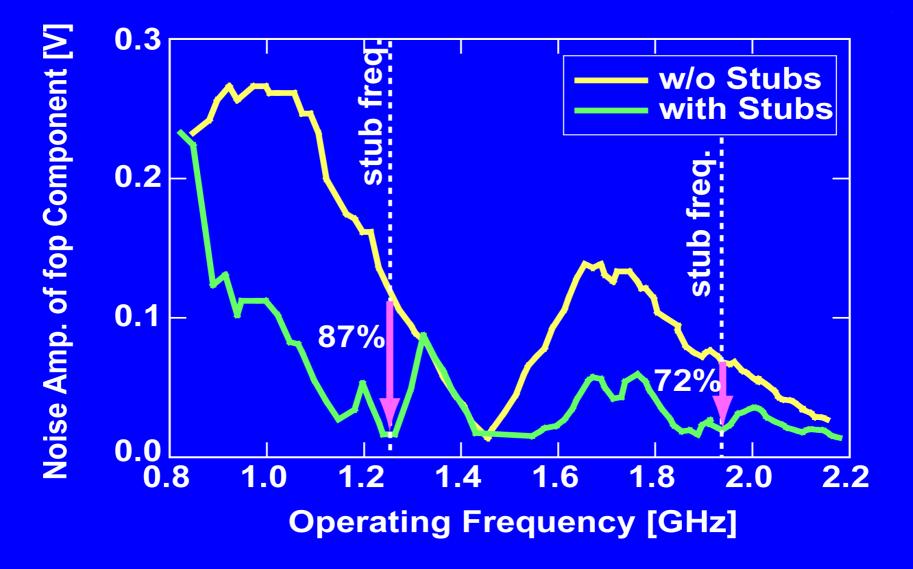
## Freq. Dependence @1.95GHz



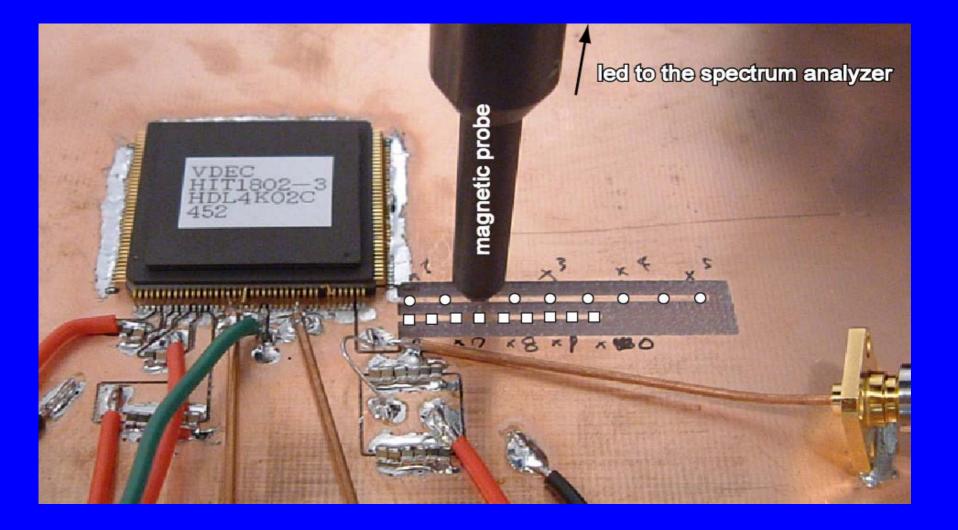
## Freq. Dependence @2.00GHz



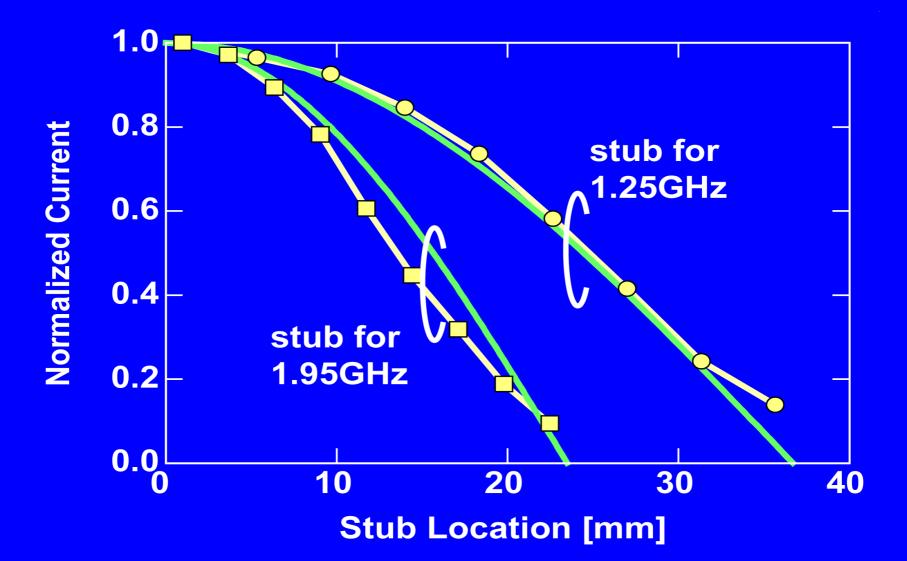
## Noise of the fop Component



## **Current Measurement**

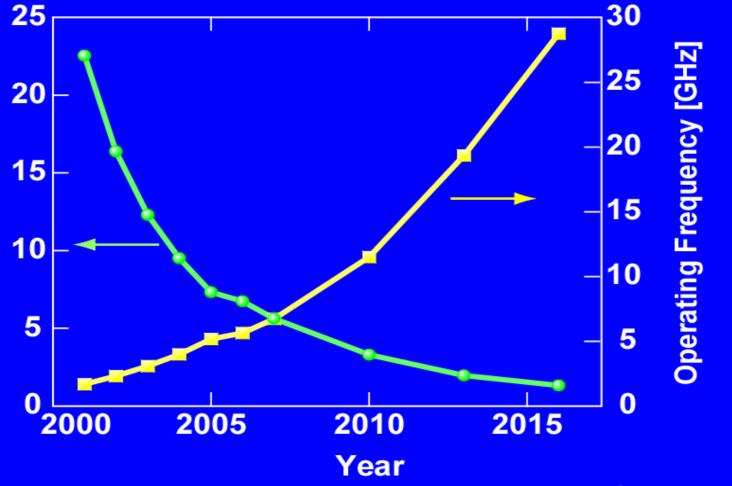


## **Current Distribution**



# **Possibility of On-chip Stub**





ITRS 2002 Roadmap

## **Short Summary**

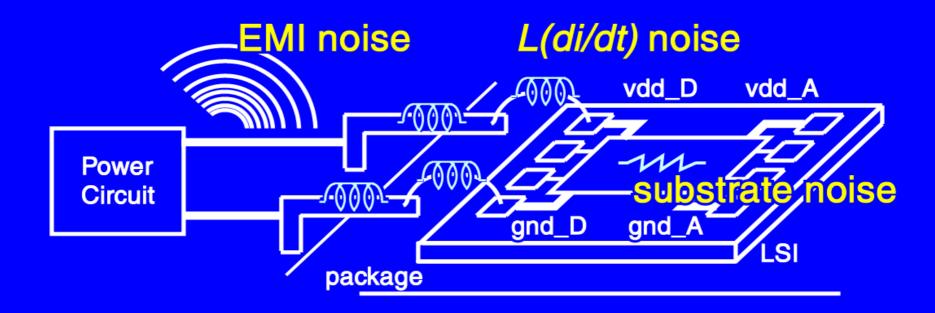
- Stub noise reduction is experimented
- The on-board stubs show clear noise reduction
  - 87%, 72% of the operating frequency component at 1.25G, 1.95GHz is suppressed
    Stub frequency dependence is observed
- On-chip stub integration will be possible in the near future

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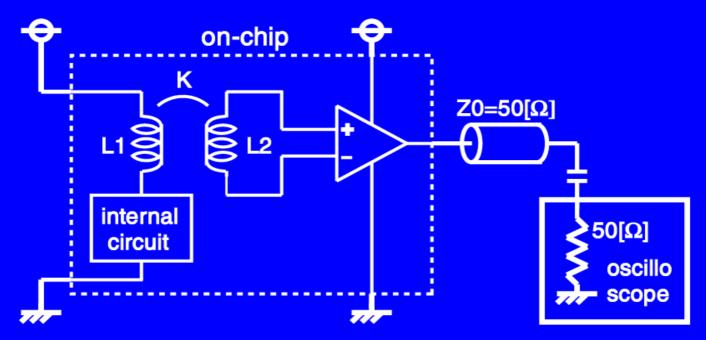
## Background

- di/dt is becoming a critical issue
- Need to measure the di/dt



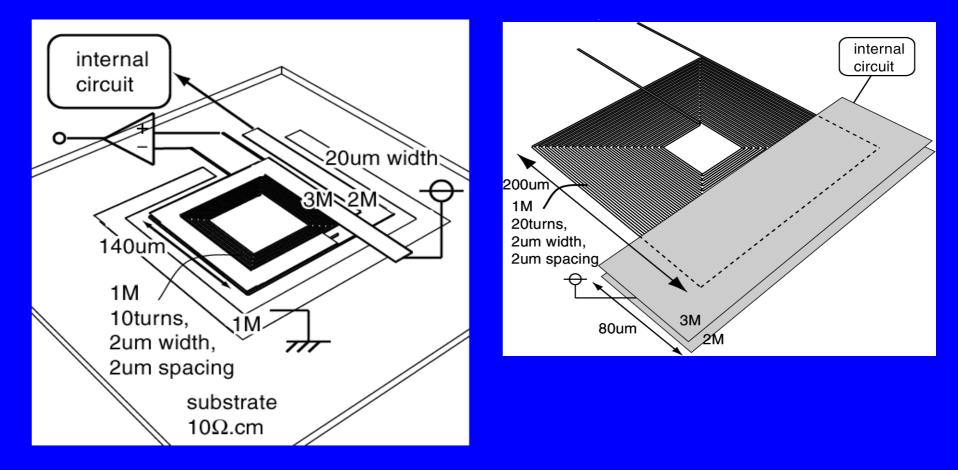
## **Block Diagram**

- L2 picks up the di/dt, induce the voltage
- Amplifier amplifies/output the voltage Pros: on-chip, real time, high-bandwidth, no numerical calculation



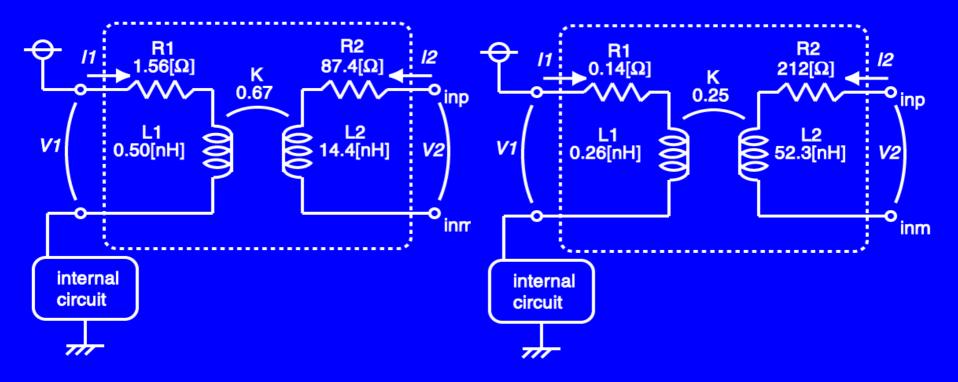
## **Improved Mutual Inductor**

#### Straight layout on the primary part



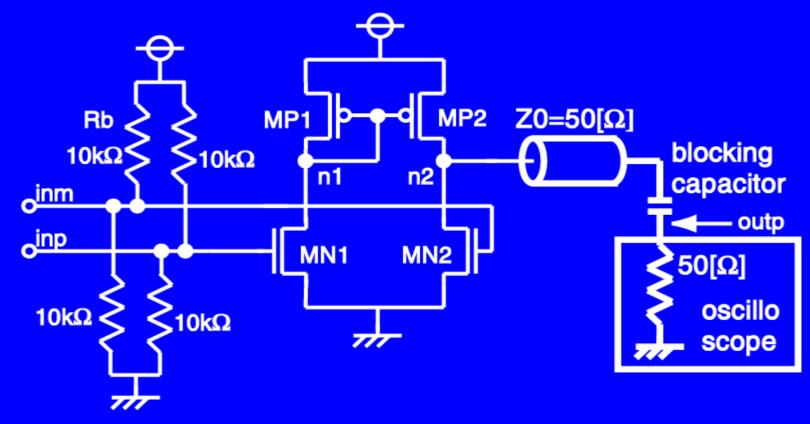
#### **Improved Mutual Inductor**

**Pros:** L1:0.5nH  $\rightarrow$  0.26nH, R1:1.56 $\Omega \rightarrow$  0.14 $\Omega$ Cons: M :1.80nH  $\rightarrow$  0.92nH (use large amp.)

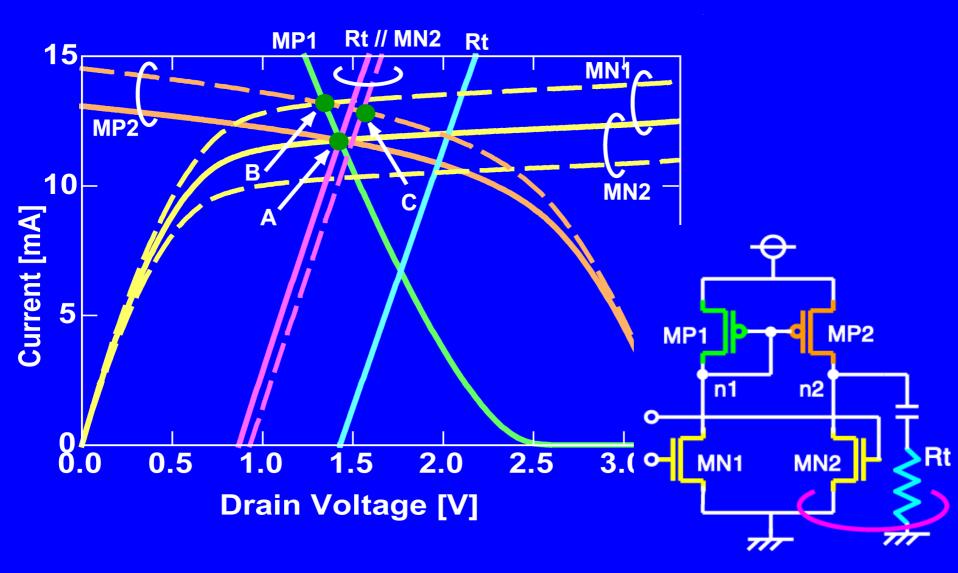


## **Amplifier/Output buffer**

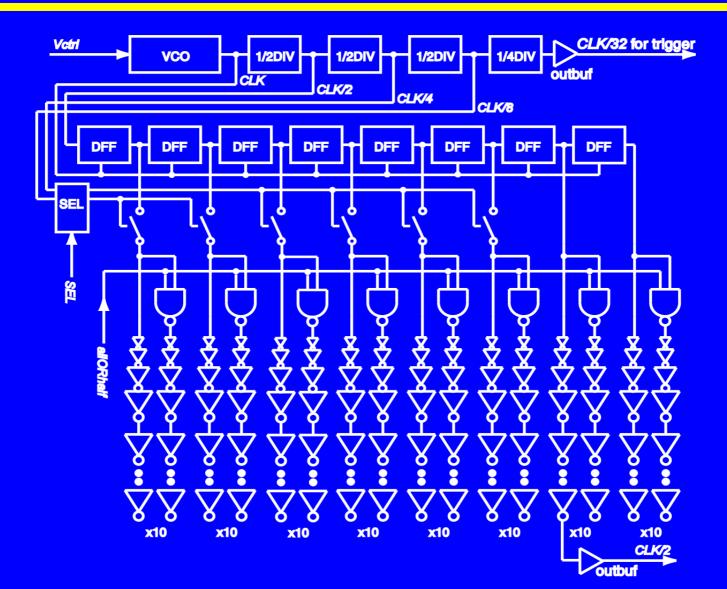
Gain: 0.76, fcut-off: 3.3GHz
 Output linearly: ±0.35V (simulation)



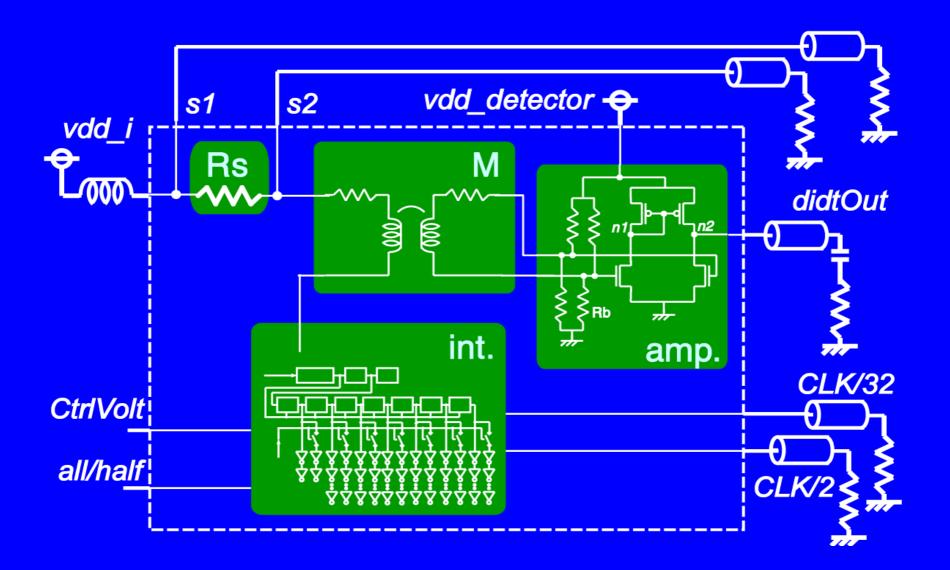
## **Bias Points of the Amplifier**



## **Internal Circuit as Noise Source**



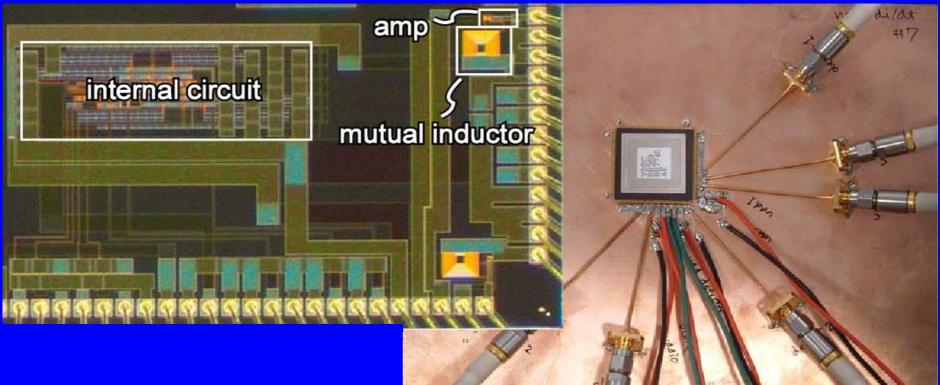
# Whole Circuit / Meas. Setup



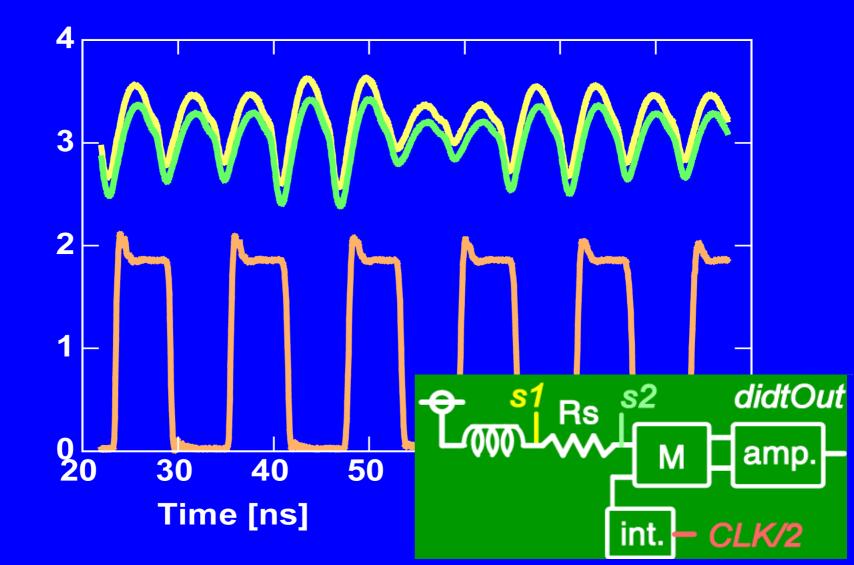
# **Chip Photograph**

#### 0.35um 3ML 2P CMOS

- Chip area : 3.0mm x 1.8mm.
- di/dt detector : 340um x 280um

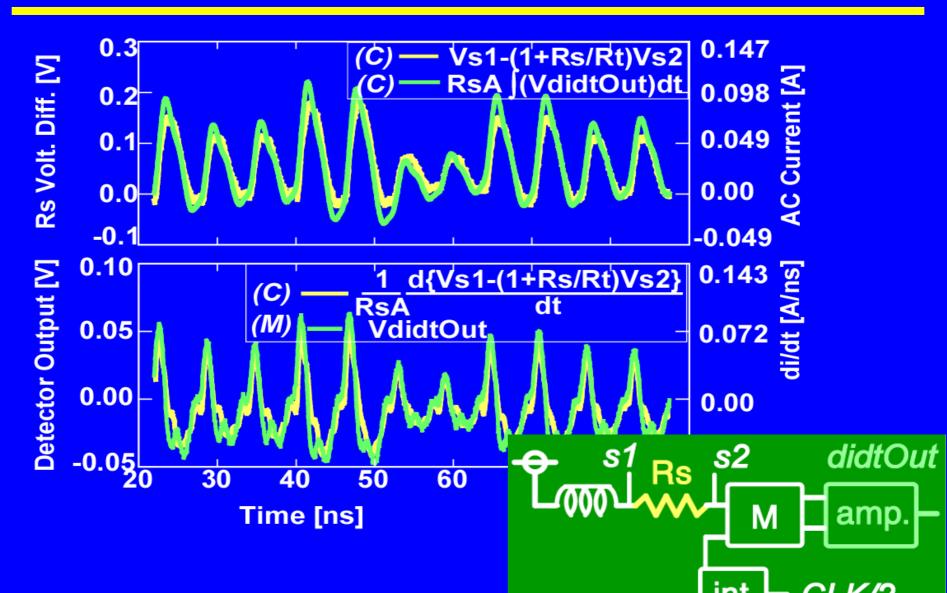


## Waveform #1

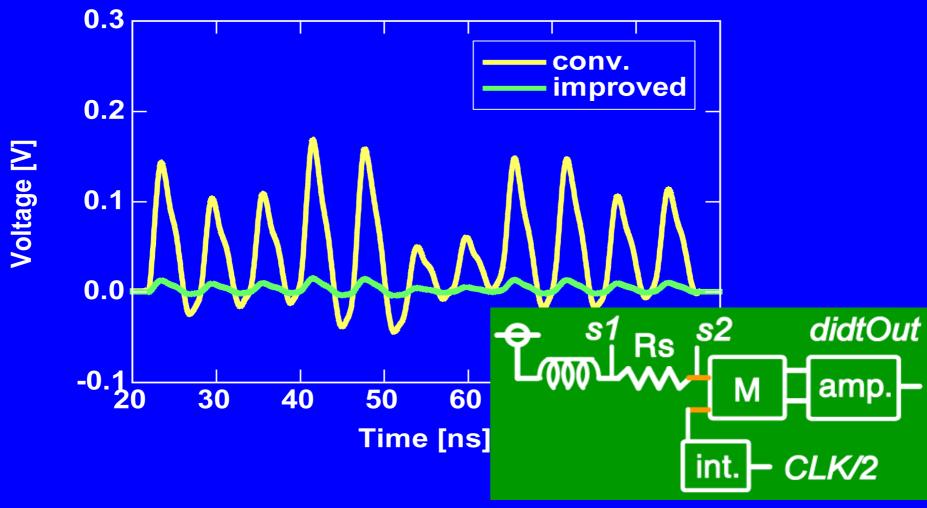


Voltage [V]

## Waveform #2



# **Voltage Drop**



Voltage drop is drastically reduced

# **Short Summary**

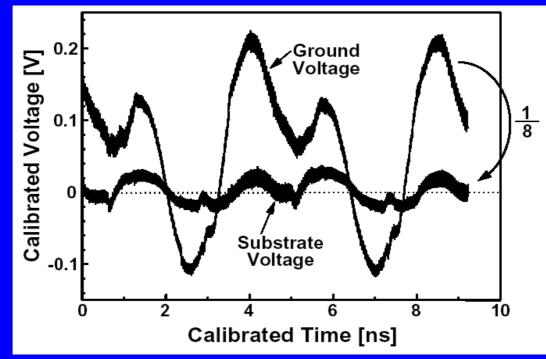
- On-chip di/dt detector is demonstrated
- It consists of a power supply line, underlying spiral inductor, an amplifier
- di/dt waveforms obtained from the di/dt detector and the resistor agree well
- Current waveform can be calculated by integrating the detector output by time
- Improved mutual inductor reduces the voltage drop

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## **Background – Substrate Noise**

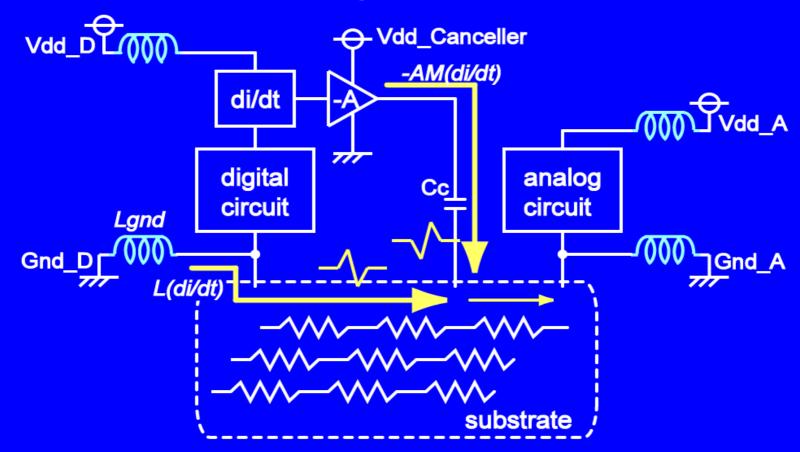
- Guard ring does not work well because of the parasitic impedance
- Substrate noise is related to Gnd noise



[16] M. Takamiya, et al. ISSCC, Feb., 2002

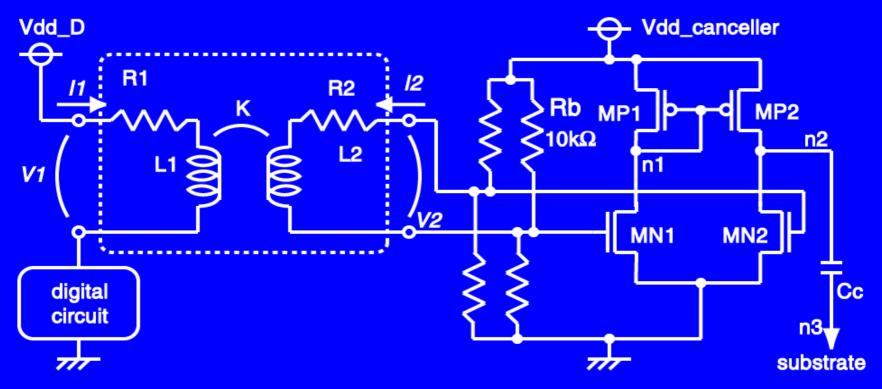
### **F.F. Active Noise Cancelling**

 di/dt detector makes anti-phase signal no feedback → high bandwidth



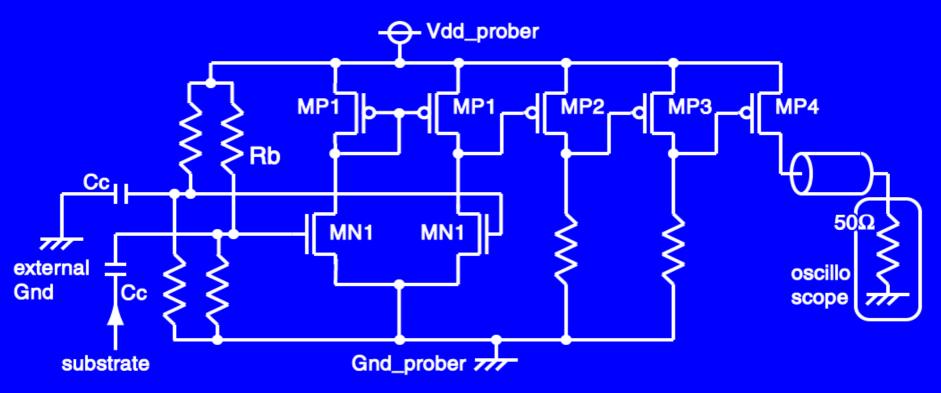
## **Noise Canceller**

- Anti-phase current should be injected
- Cc is large so as to adjust the phase of the original noise and injected currents

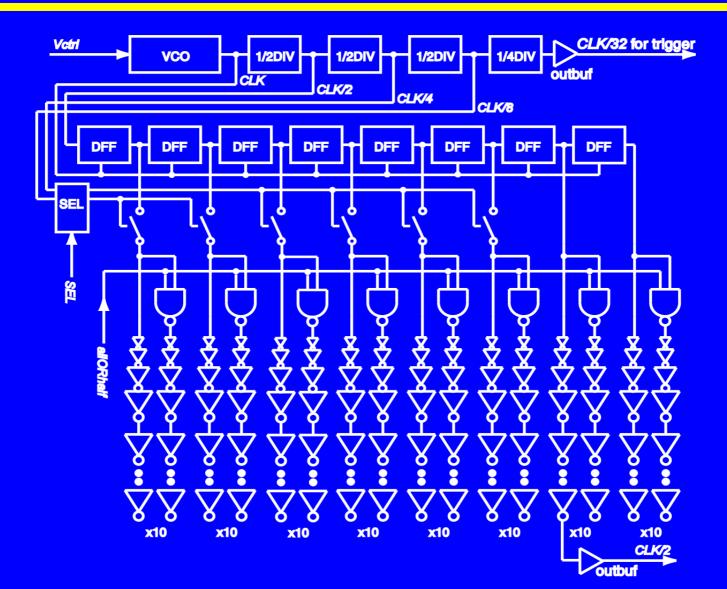


# **Noise Probing for Verification**

- Differential amplifier connected to the substrate and the external Gnd
- No body contact for NMOS (gm/gbs=6.0)

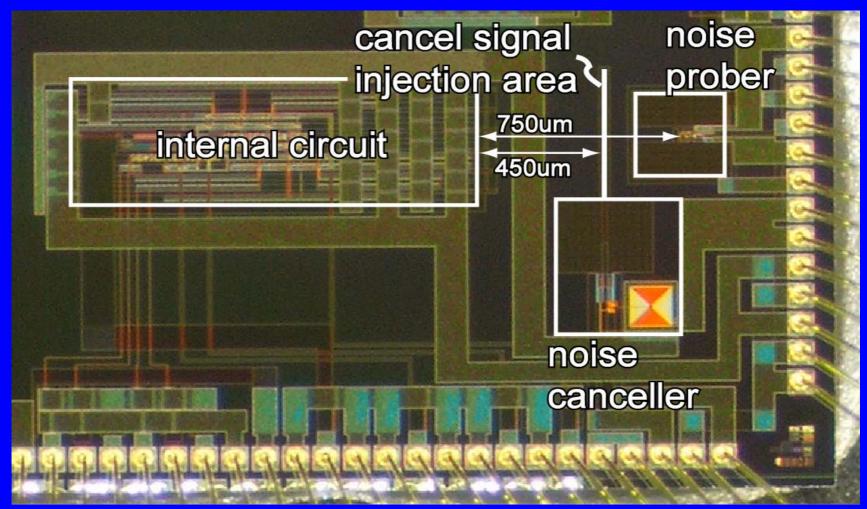


## **Internal Circuit as Noise Source**



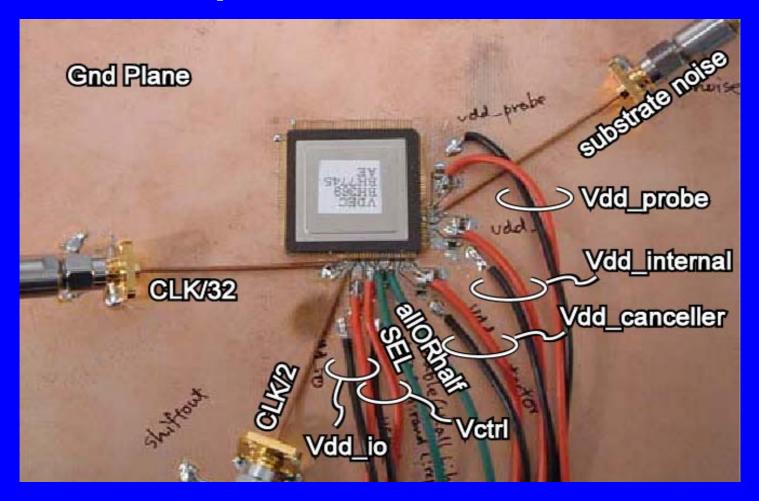
# **Chip Photograph & Floor Plan**

### 0.35um 3ML 2P CMOS (3.0mm x 1.8mm)

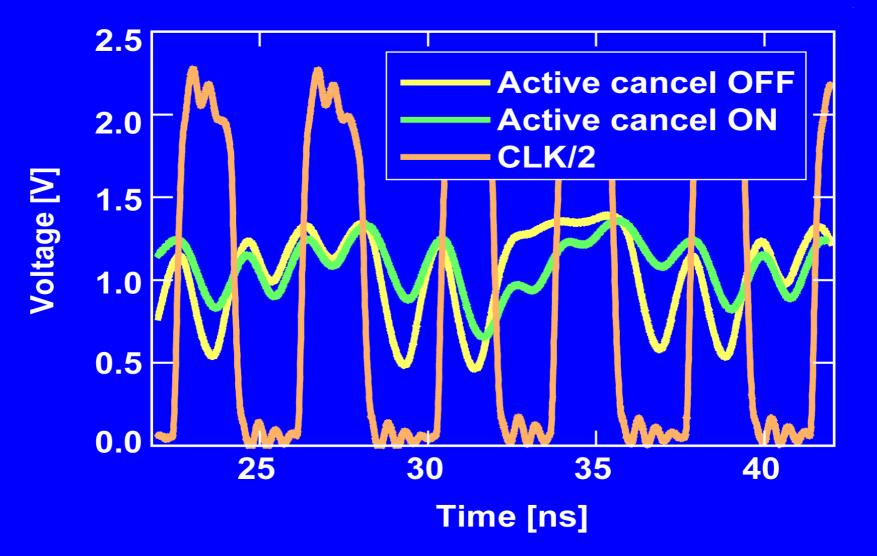


## **Chip Mount**

#### The test chip is mounted on a Cu board

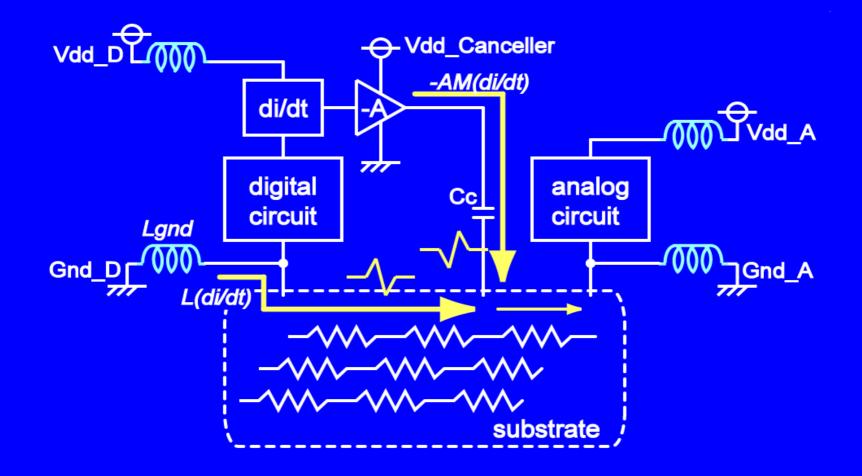


# Waveform (Random@500MHz)

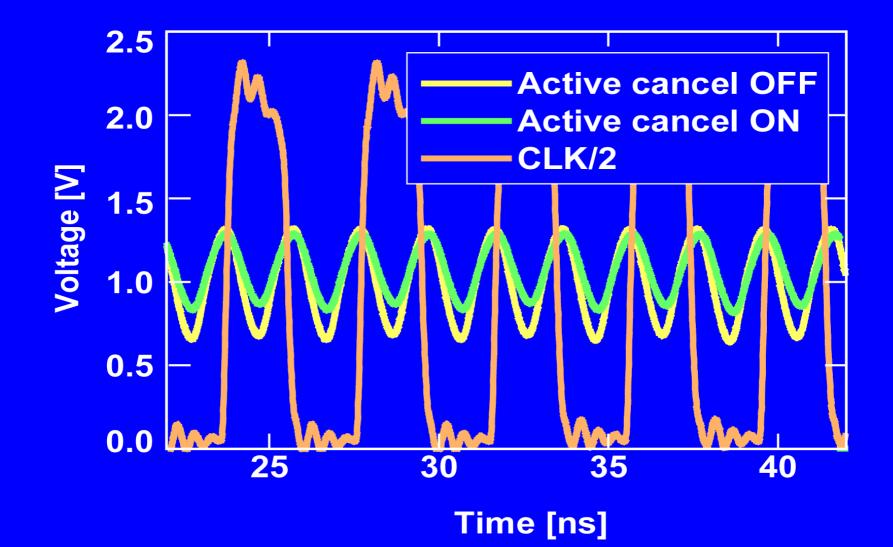


### **Active Cancel ON/OFF**

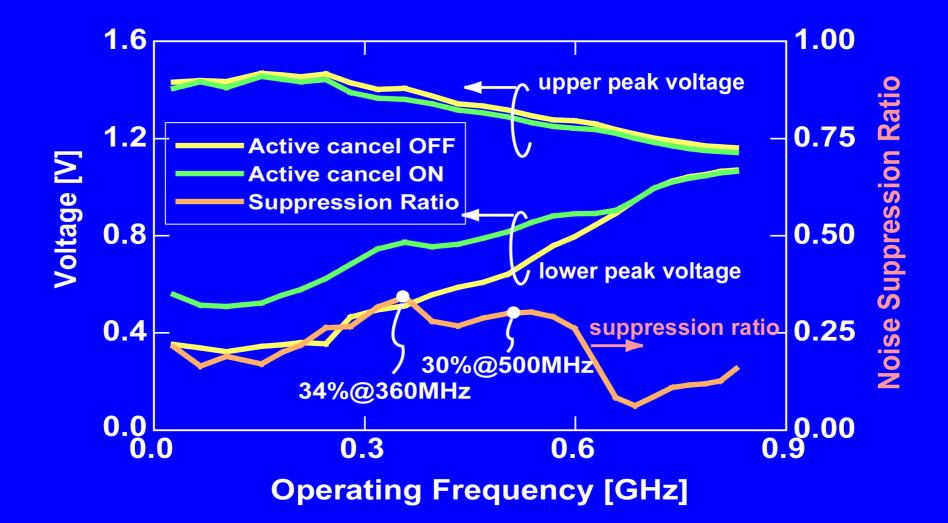
#### ON, OFF means Vdd\_Canceller=3.3V, 0V



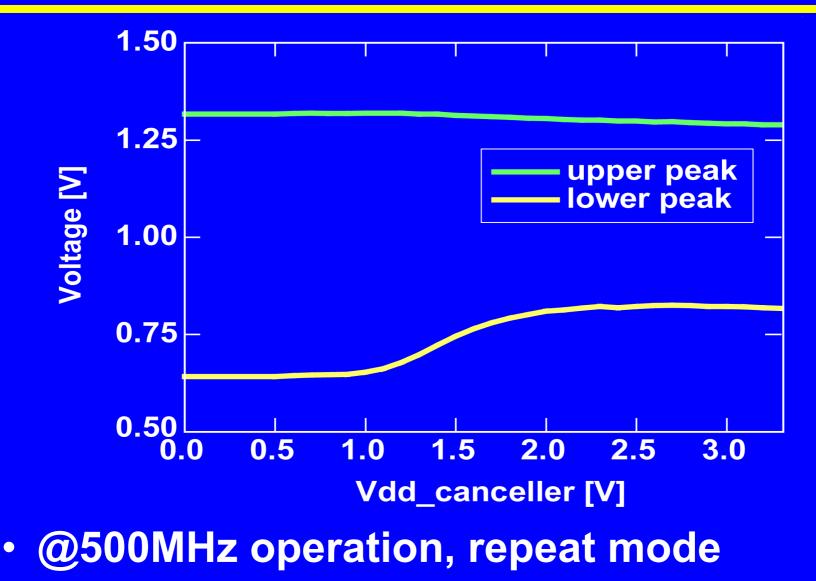
# Waveform (Repeat@500MHz)



# Frequency Dependence (repeat)

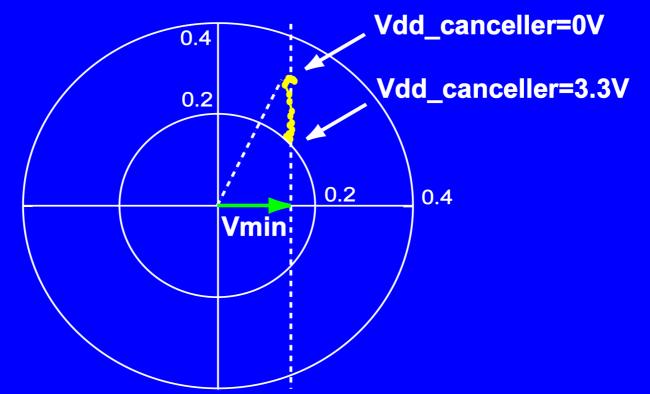


## **Noise Amplitude Change**



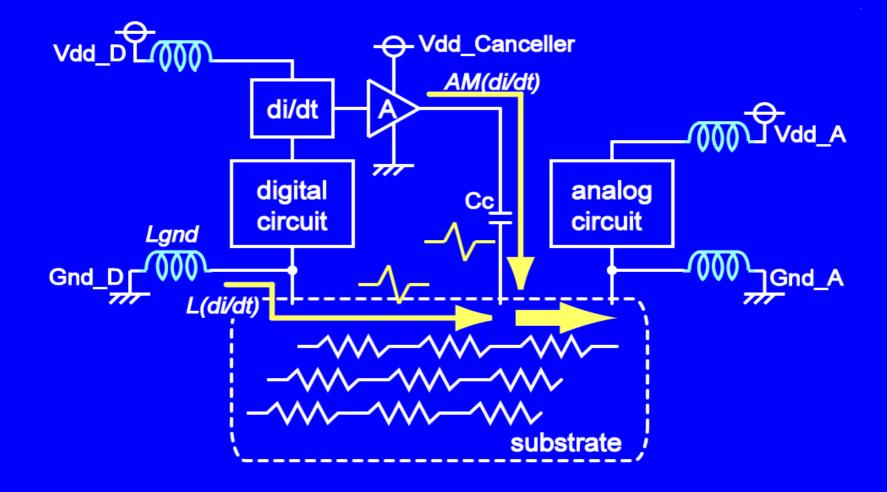
## **Phasor of the Substrate Noise**

- Phase of the injected current is  $-\pi/2$
- 54% noise reduction would be achieved by optimizing the amplifier design

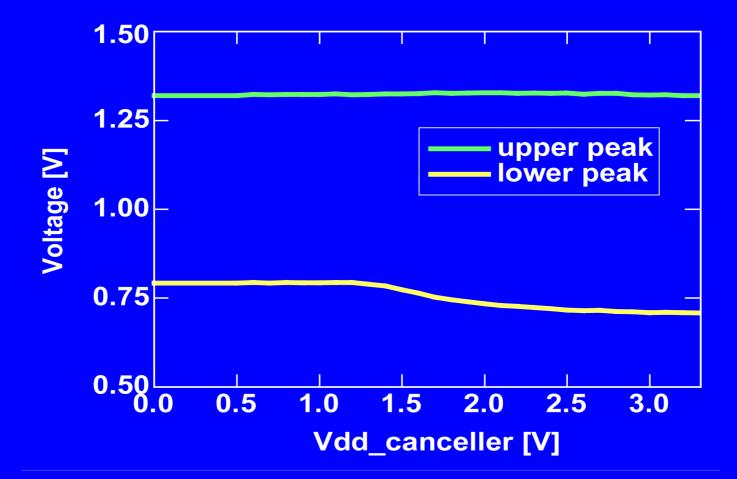


## **In-phase Current Injection**

#### In-phase injection increase the noise



## **In-phase Current Injection**



This result supports our model

# **Short Summary**

- Feedforward active substrate noise cancelling technique is demonstrated
- A di/dt detector generates anti-phase signals, and injected into the substrate
- Measurement results show that 17% to 34% of the substrate noise reduction is achieved from 100MHz to 600MHz range
- Optimized injector design will enhance the noise suppression ratio up to 56%

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## Conclusions

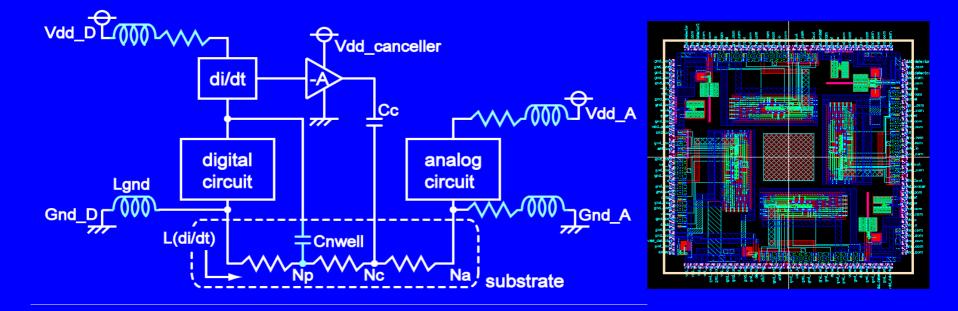
- Stubs and capacitors are compared for power supply noise reduction
  - Boundary frequency is clarified
  - Stubs have advantage for high-frequency
- Clear supply noise reduction effects were observed with on-board stubs
- On-chip di/dt detector was demonstrated – on-chip and real time di/dt measurement
- Feedforward active substrate noise cancelling was demonstrated

   Use the di/dt detector



# Future Works (1/4)

 Measure the substrate noise cancelling circuit (chip delivery 10/8)



# Future Works (2/4)

 Measure an improved di/dt detector **Pros:** L1:0.5nH  $\rightarrow$  0.26nH, R1:1.56 $\Omega \rightarrow$  0.25 $\Omega$ Cons: M :1.80nH → 0.92nH - Depend on the delivery date (10/8???) internal circuit **R2** R1 1.56[Ω] 12 87.4[Ω] Κ 0.67 inp L1 0.50[nH] L2 14.4[nH] V1 V2 200um 1M 20turns, inm 2um width. 2um spacing

> internal circuit

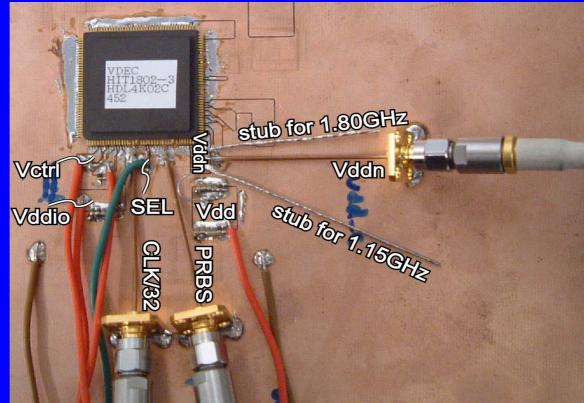
80um

3M

# Future Works (3/4)

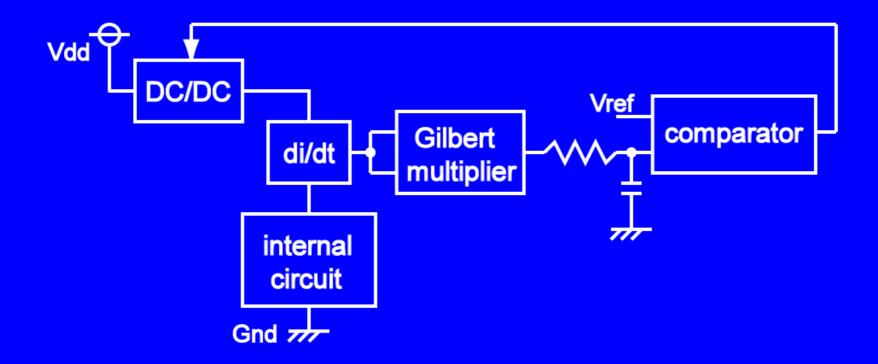
### Off-chip stub vs off-chip capacitor

#### Write stub and capacitor patterns with the same area on PCB



## Future Works (4/4)

#### Simulate a feedback di/dt control system



# Introduction

# **Power Supply Noise**

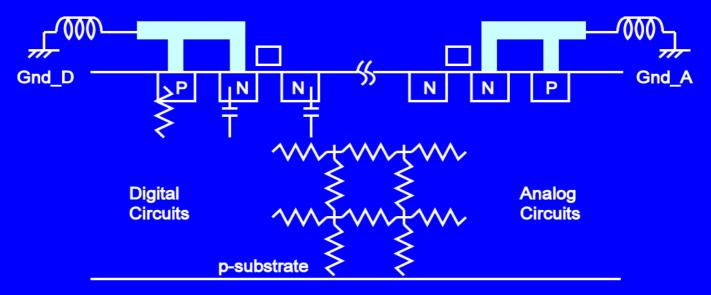
- As the Vdd decrease, the noise margin is reduced
  - Timing violation *delay ~ 1/(Vdd-Vth)*
  - Logic error
- L(di/dt)+RI causes the noise
  - L(di/dt) is dominant in high-speed LSIs
  - Decoupling capacitor reduce the di/dt
    - Requires more die area for on-chip capacitor
    - Parasitic inductance disturbs for off-chip capacitor

# **Power Supply Noise**

- As the Vdd decrease, the noise margin is reduced
  - Timing violation delay ∝ 1/(Vdd-Vth)
  - Logic error
- L(di/dt)+RI causes the noise
  - L(di/dt) is dominant in high-speed LSIs

## **Substrate Noise**

- PLL jitter becomes 10 times bigger by the substrate noise [16]
- Coupling from power supply noise is the main source → di/dt is important



[16] P. Larsson, JSSC July 2001

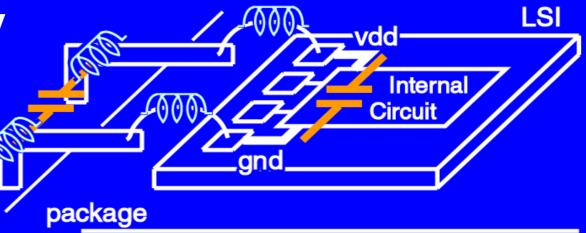
### EMI noise

- EMI radiation can cause operational problems in other devices
- EMI radiation occurs from cables, connectors, PBC, package ...
- Ultimate noise source is di/dt caused by gate switching in LSIs
- EMI radiation is caused by di/dt, not by voltage perturbation

Theoretical Study of Stubs vs Capacitors

# Background

- Decoupling capacitor
  - Area penalty
  - Parasitic
    - inductance

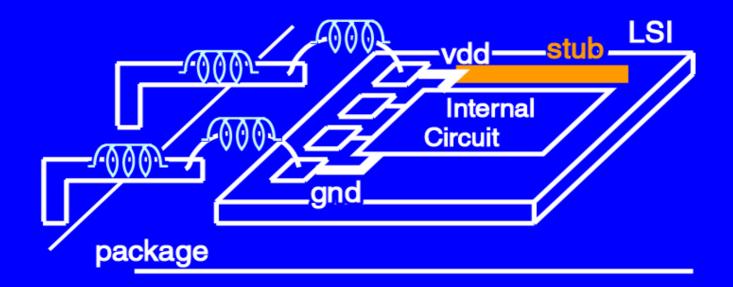


- Semi-asynchronous architecture

   Complicated design
- Spiral power line on PCB board – Complicated design

# **Power Line Noise Reduction**

 Attach the stub to the power line will reduce the power supply noise

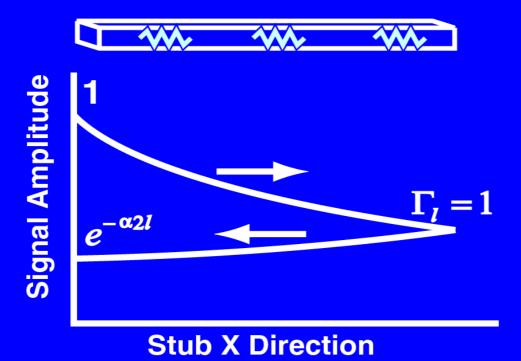


#### **Stub Theorem**

- Input impedance of the transmission line of Z0,  $\beta$ , I, and ZL termination :  $Zstub = Z_0 \frac{ZL \cos\beta I + ZO \sin\beta I}{ZO \cos\beta I + ZL \sin\beta I}$
- When open termination (ZL=infty)  $Zstub = Zo \frac{cos\beta I}{j \sin\beta I}$
- When the line length is quarter of the wavelength (βI=π/2), no loss (R=G=0)
   Zstub = 0

### **Stub Resistance**

- The resistance of the stub degrade the noise reduction effect
  - Round trip attenuation factor  $\eta = e^{-\alpha 2I}$

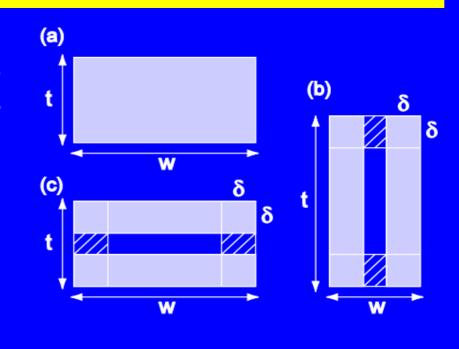


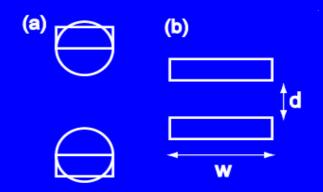
# **Transmission Line Parameters**

*2*ρ

δ=

- Resistance
   Skin effects
- Capacitance
   Parallel plate
  - for d<w
  - Parallel cylinder for w<d</li>
- Inductance
  - $-c^2/\epsilon_r = 1/LC$





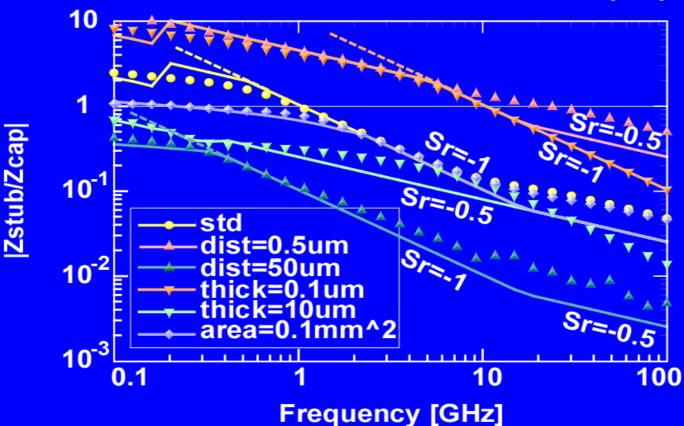
### **Boundary Frequency**

- Stub input impedance  $Zstub \propto f^{-2}$ ,  $f^{-1.5}$  $-I \propto f^{-1}$ ,  $w \propto f$ ,  $\delta \propto f^{-0.5}$ , Zstub=RI/2
- Capacitor input impedance Zcap ∝f<sup>-1</sup>
- Boundary frequency at Zstub=Zcap

$$fB = \frac{\pi c^2 \varepsilon_0 \rho}{8td} \qquad \frac{t^3}{A} < \frac{16\rho\sqrt{\varepsilon_r} \varepsilon_0 c}{\pi} \quad \text{and} \quad t < \frac{16d}{\pi^2}$$
$$\frac{t^3}{A} > \frac{16\rho\sqrt{\varepsilon_r} \varepsilon_0 c}{\pi} \quad \text{and} \quad t > \frac{\pi^3 c \sqrt{\varepsilon_r} \varepsilon_0 \rho A}{64d^2}$$
$$fB = \frac{\pi^3 c^2 \varepsilon_0 \rho}{256d^2} \quad \frac{t^3}{A} < \frac{16\rho\sqrt{\varepsilon_r} \varepsilon_0 c}{\pi} \quad \text{and} \quad t > \frac{16d}{\pi^2}$$
$$\frac{t^3}{A} > \frac{16\rho\sqrt{\varepsilon_r} \varepsilon_0 c}{\pi} \quad \text{and} \quad t > \frac{\pi^3 c \sqrt{\varepsilon_r} \varepsilon_0 \rho A}{64d^2}$$

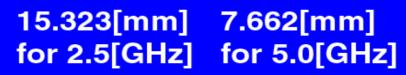
# **Numerical Analysis**

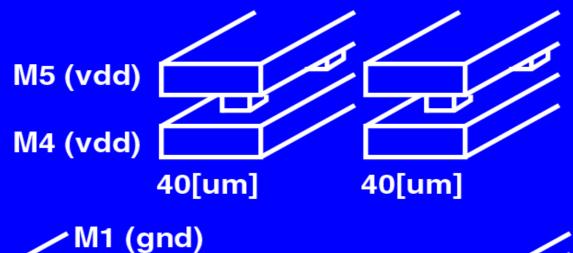
- Raphael(L,C), Fasthenry(R) vs. the model
- d=5um, t=1um, A=1mm<sup>2</sup>, εr=3.9, ρ=ρCu



#### **Stub Structure**

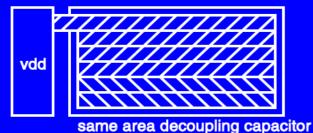
- 0.18um 5M CMOS of company "H"
- For a 2.5GHz operation circuit





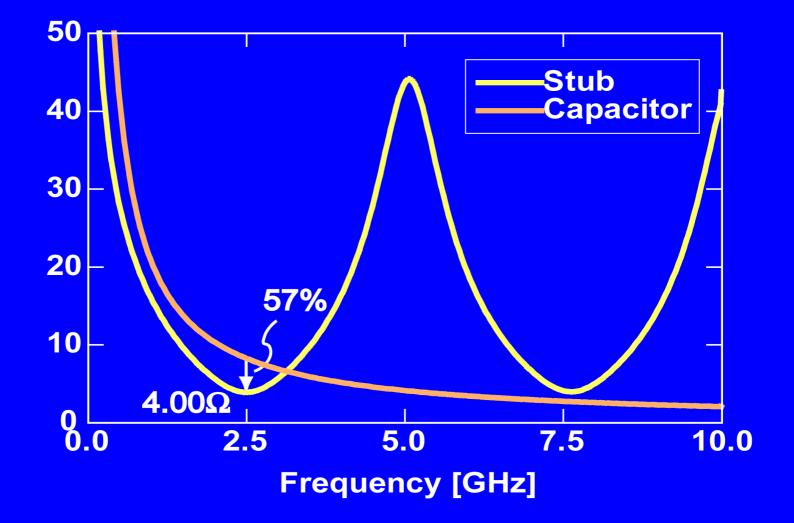
# **Stub and Same-Area Capacitor**





# Stub Input Impedance vs. Freq



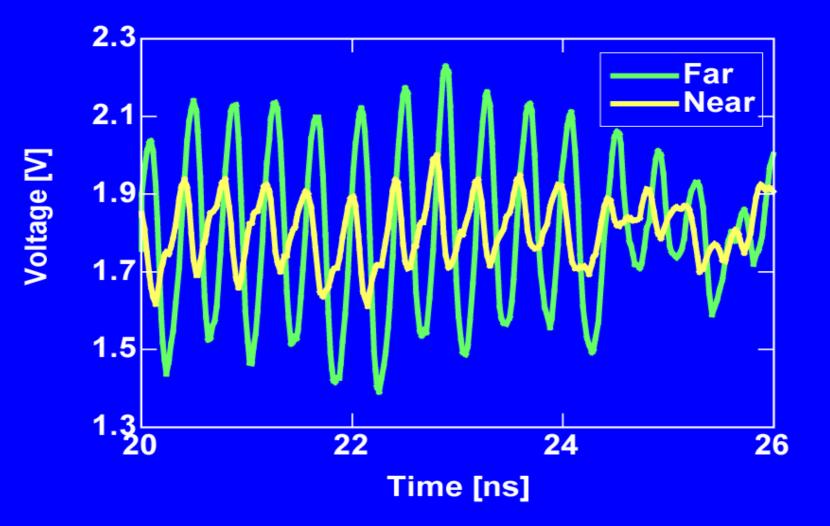


# **Voltage Swing at Far End**

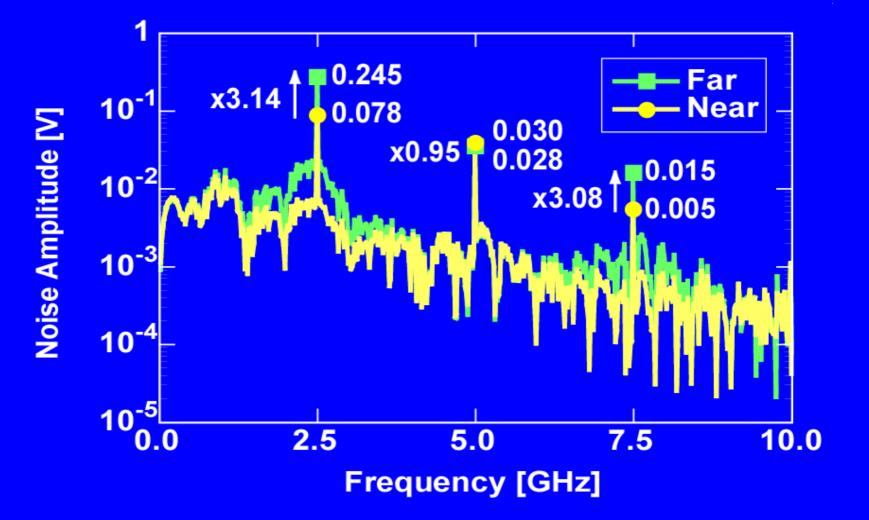
The voltage swing at far end is bigger

$$(0) (4T/8) (8T/8) (9T/8) (9T/8) (9T/8) (9T/8) (9T/8) (9T/8) (10T/8) (10T/8) (11T/8) (11T/8)$$

## Waveform of Near/Far End



# **Spectrum of Near/Far End**

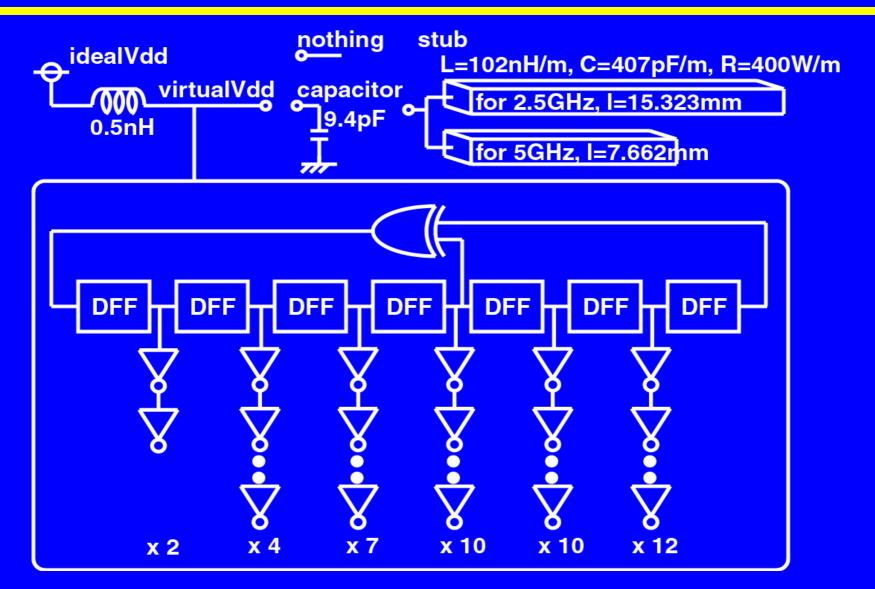


# **Stub Design**

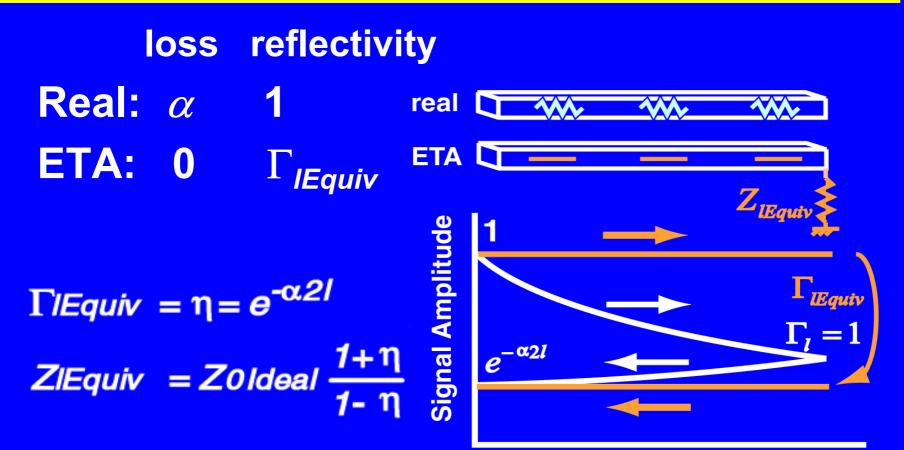
- Stub length: quarter wavelength of the operating frequency
  - Stub input impedance has frequency dependence
  - Operating frequency is the dominant component of the power supply noise
- Width: Wider is better for noise reduction

   Smaller resistance, (bigger capacitance)
- Target of this study
  - Observe the noise difference between a stub and the same space decoupling capacitor

## **Test Circuit**

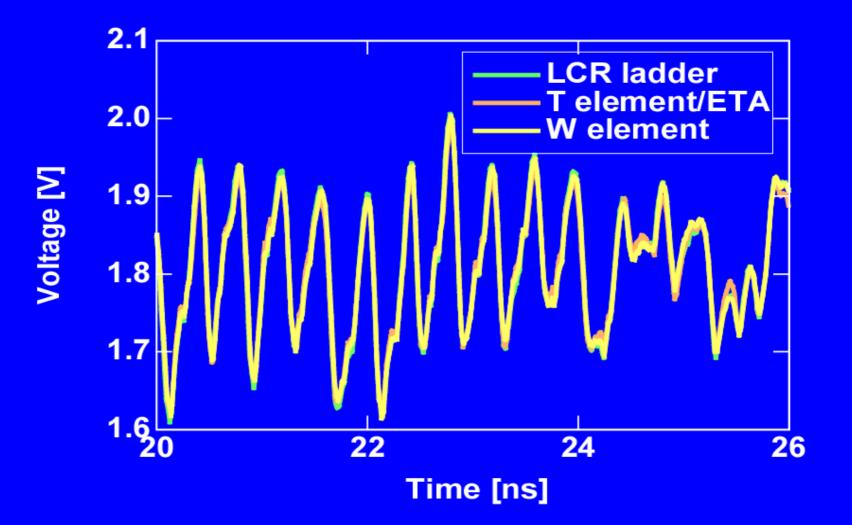


# **Equivalent Termination Approx.**



**Stub X Direction** 

## **ETA Waveforms**



# Analytical Models using ETA (1)

The stub input impedance

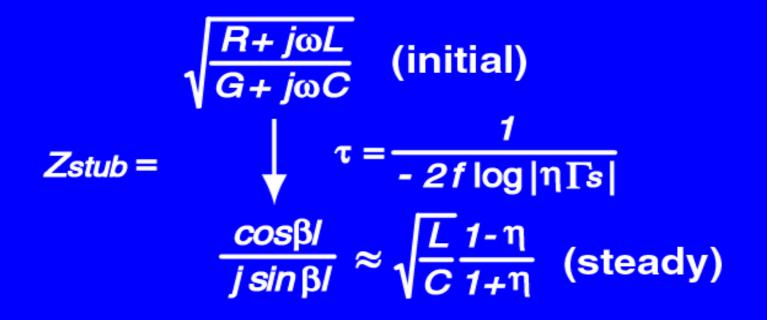
 $ZstubEquiv = \sqrt{\frac{L}{C}} \frac{1-\eta}{1+\eta}$ 

The voltage ratio of the near and far end

$$\frac{V far}{V near} = -j \frac{1+\eta}{1-\eta}$$

# **Analytical Models using ETA (2)**

- Time constant for stub impedance change
  - At the initial state, stub input impedance is the same as the characteristic impedance

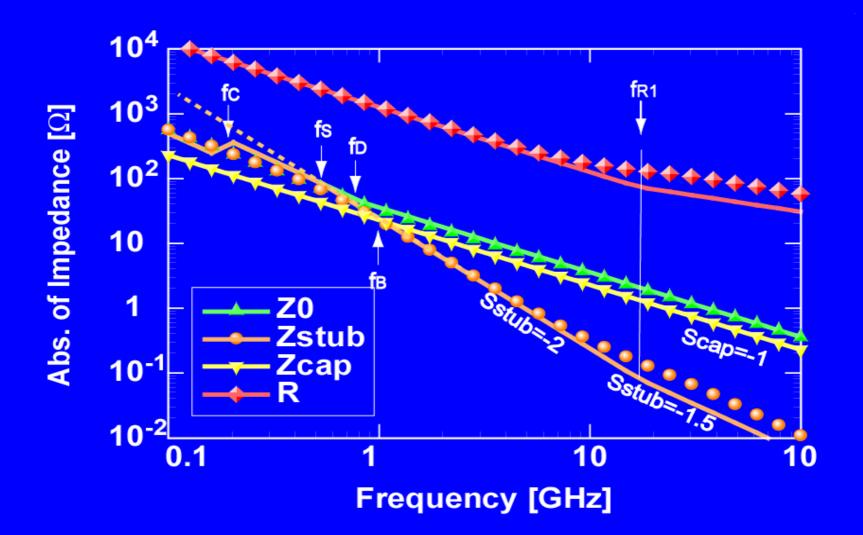


# **Lump or Distributed Element?**

Signal propagation time through a wire, ulletcompared with the cycle time: Negligibly small  $\rightarrow$  lump element (R, C ladder) → distributed element Comparable (transmission line)  $Z_0 = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$ , length

 $\beta_c = -j\sqrt{(R+j\omega L)(G+j\omega C)} = \beta_r - j\alpha$ 

# **Numerical Analysis**

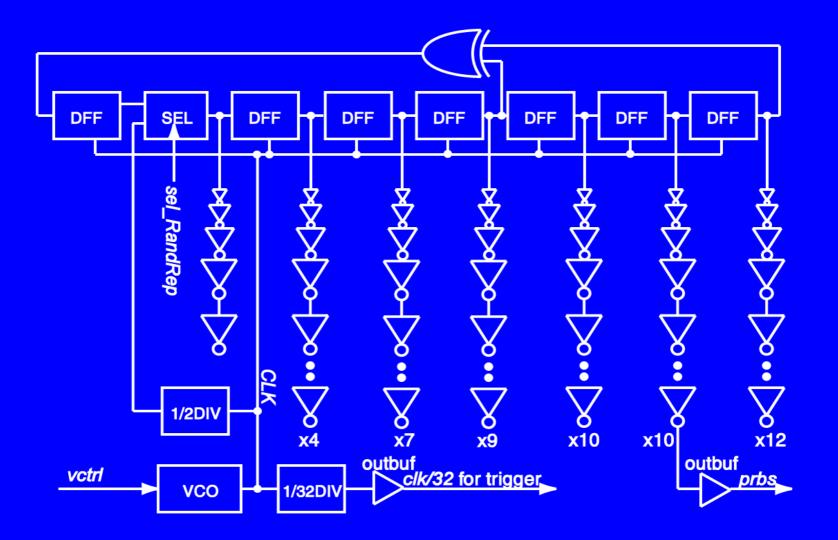


# **Stub Measurement**

# Background

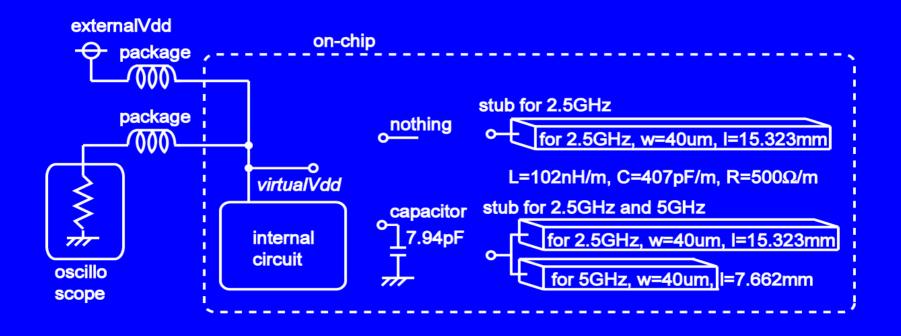
- Theoretical study predicts that stubs can reduce the power supply noise better than decoupling capacitor
- Let's verify the stub noise reduction by experiments

## **Internal Circuit**



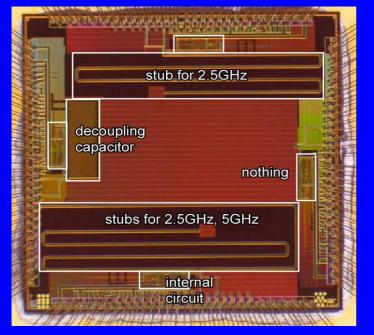
## **Power Line Structures**

 nothing, capacitor, stub for 2.5GHz, stub for 2.5GHz and 5GHz



# **On-chip Stub Does Not Work**

- 0.18um 5ML standard CMOS (5.9mm x 5.9mm)
- The chip is mounted on a Cu board

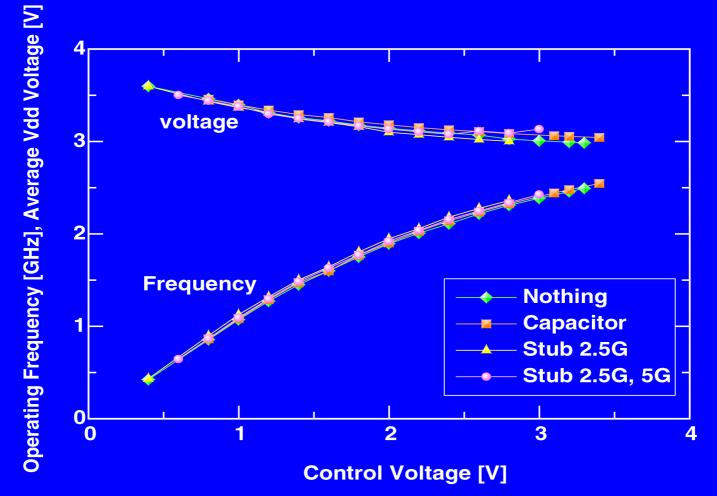




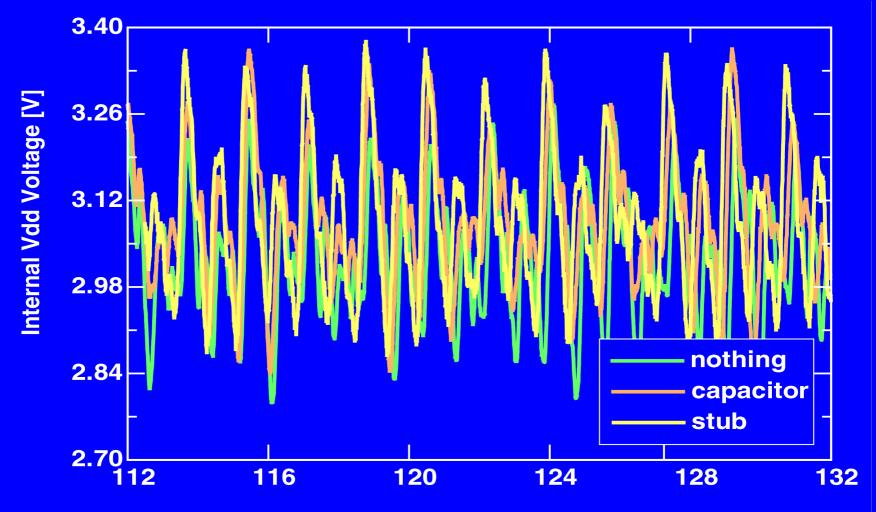
- Reflection at the bent (length>15mm @2.5GHz)
- Resistance is bigger than the estimated value

## VCO characteristics, IR drop

#### Intra-chip fluctuation is small



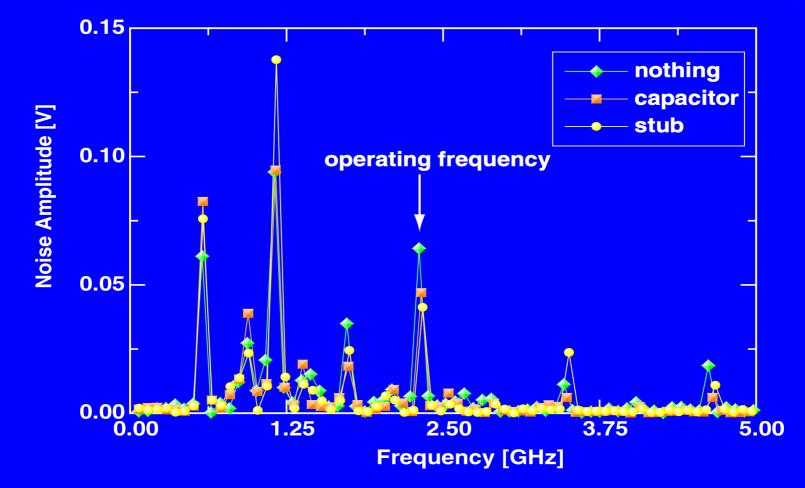
#### **Measured Vdd Waveforms**



Time [ns]

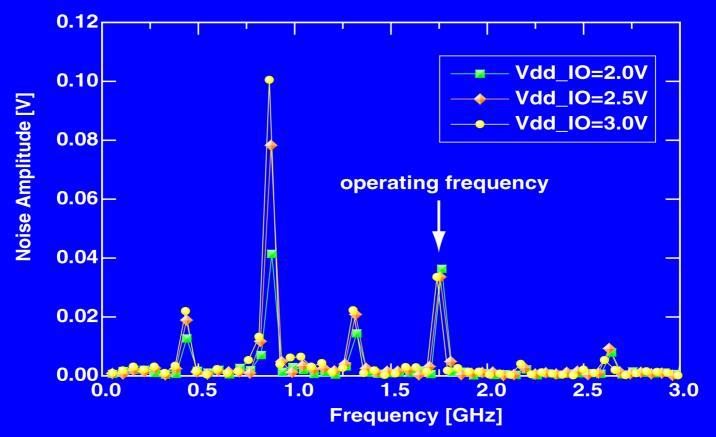
#### **Measured Vdd Spectrum**

#### Noise peak at f/2, f/4



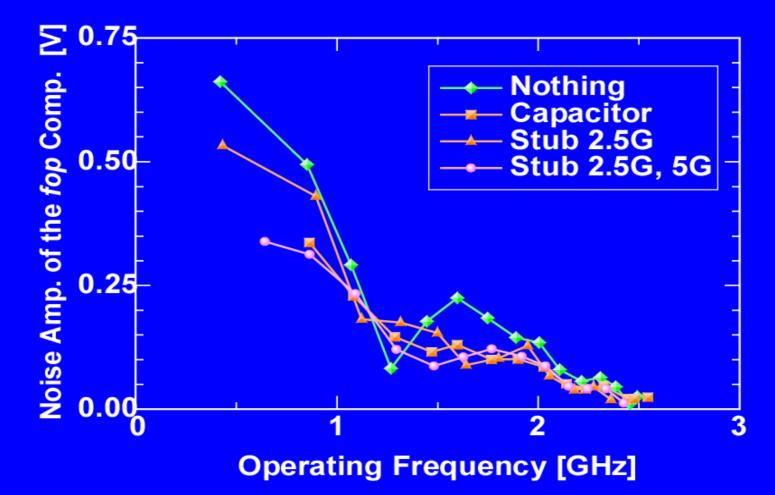
# VddIO dependece of Vdd Noise

 Substrate/package coupling of Vdd-IO and Vdd-core



# **Operating Freq. vs. Noise**

The difference is not clear

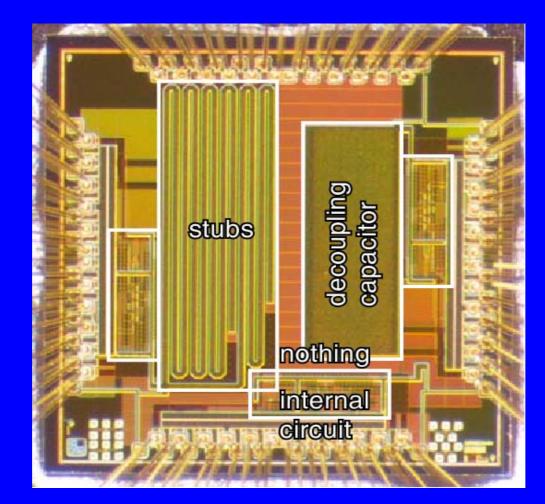


# Why the Difference is Small?

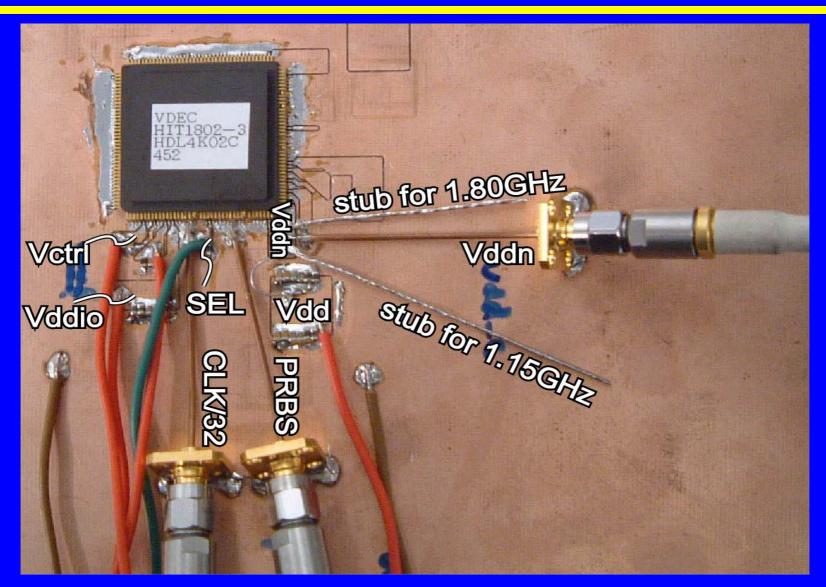
- Stubs are bent in the chip and reflection occurs
- The resistance is much bigger than the estimated value
  - The provided resistance value seems to be a measured sheet resistance at DC
- Package impedance is so big that the noise signal cannot come out

# **Chip Photograph**

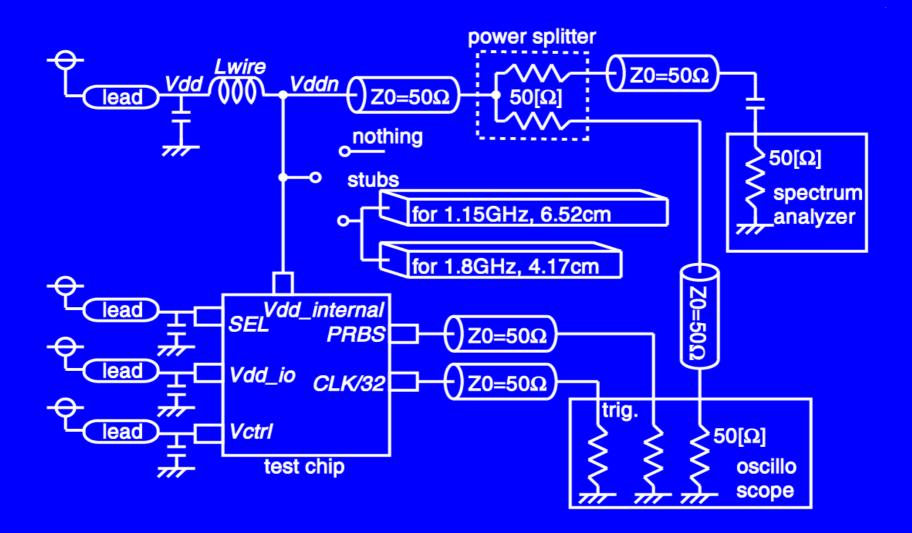
#### • 0.18um 5ML CMOS (2.4mm x 2.4mm)



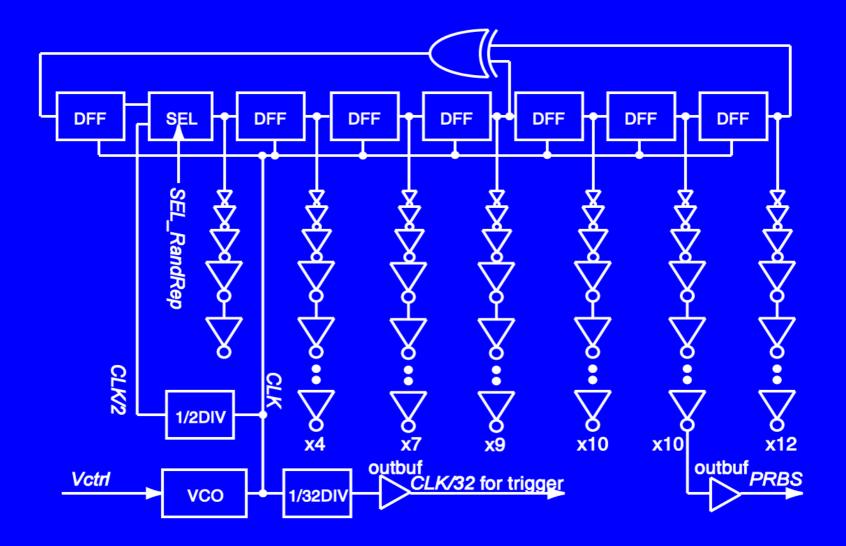
## **Off-chip Stubs**



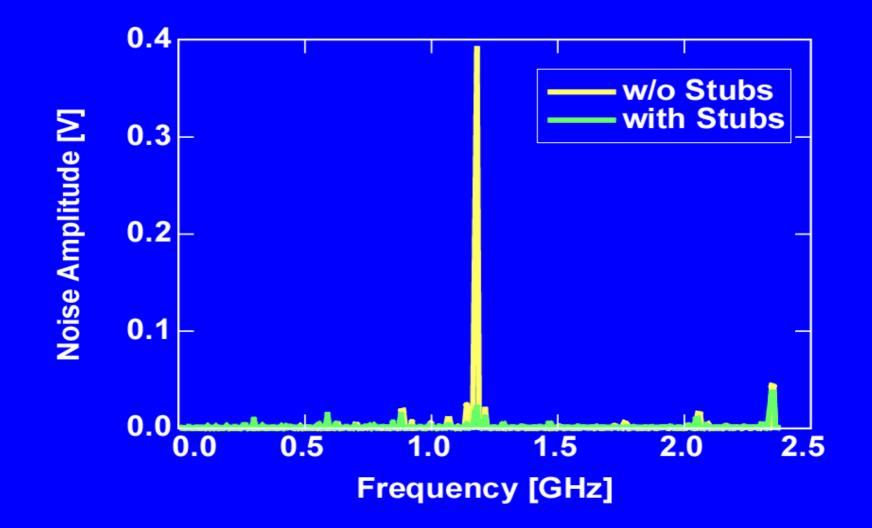
#### **Schematic**



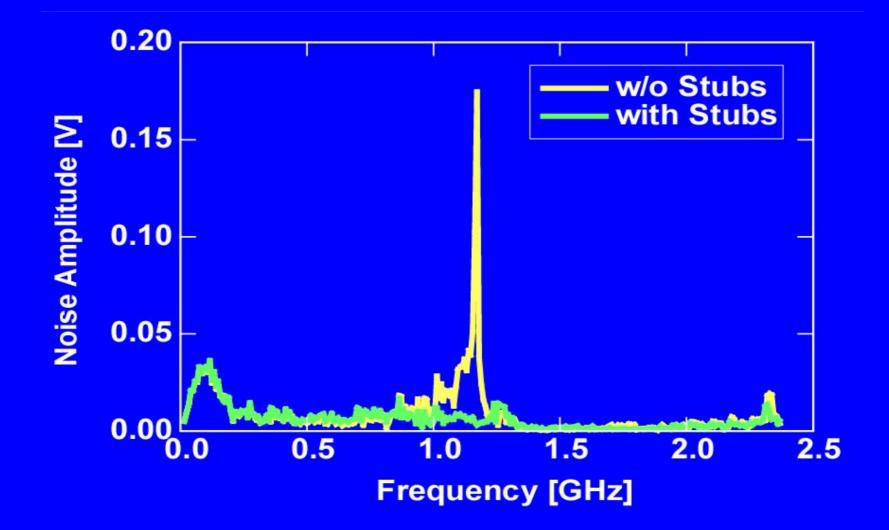
## **Internal Circuit**



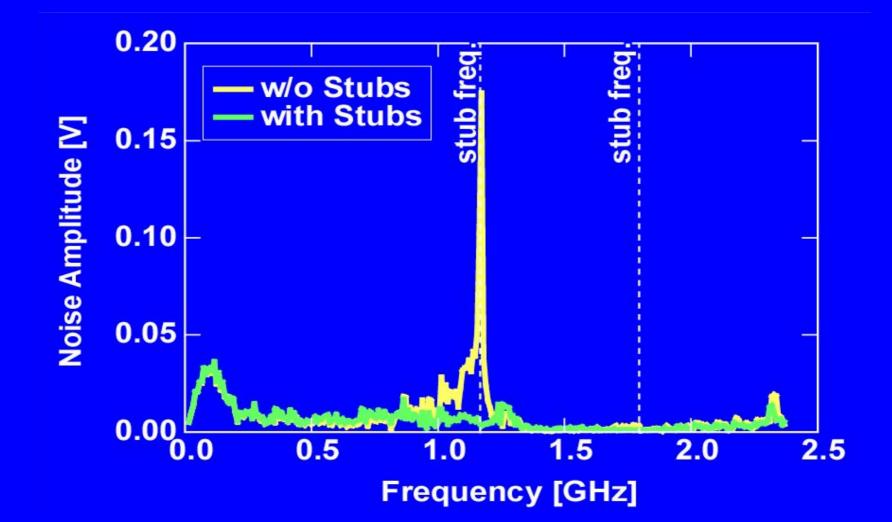
## Spectrum @1.15GHz Repeat



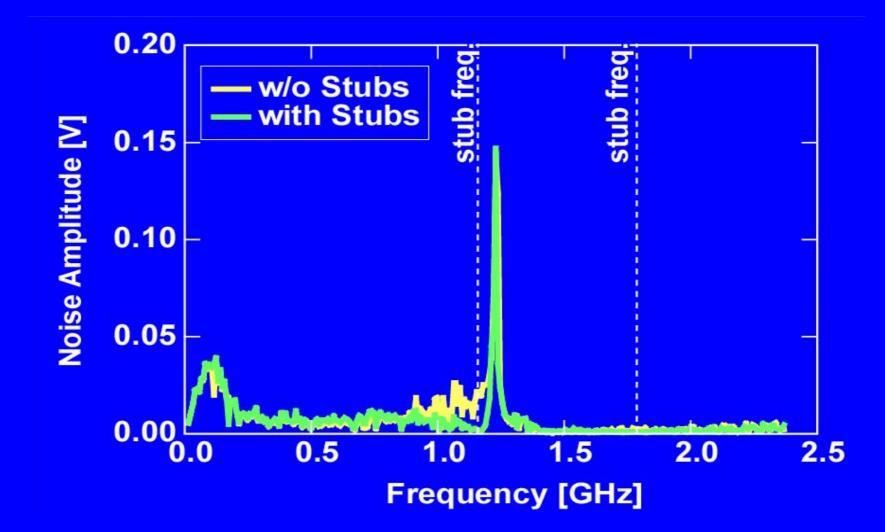
# Spectrum @1.15GHz Random



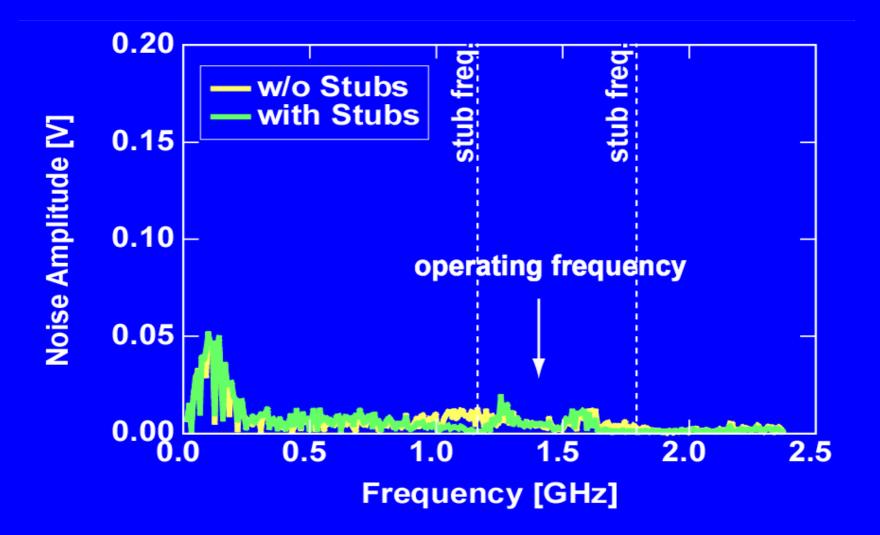
# Freq. Dependence @1.15GHz



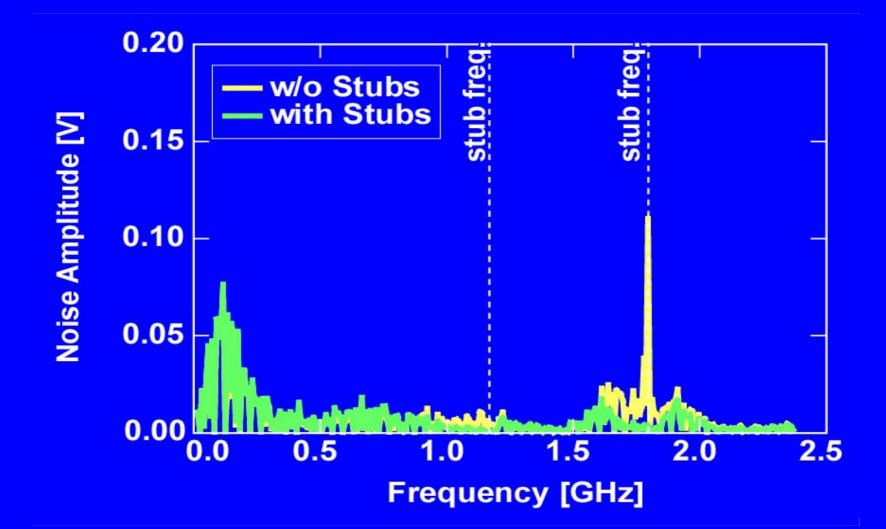
# Freq. Dependence @1.25GHz



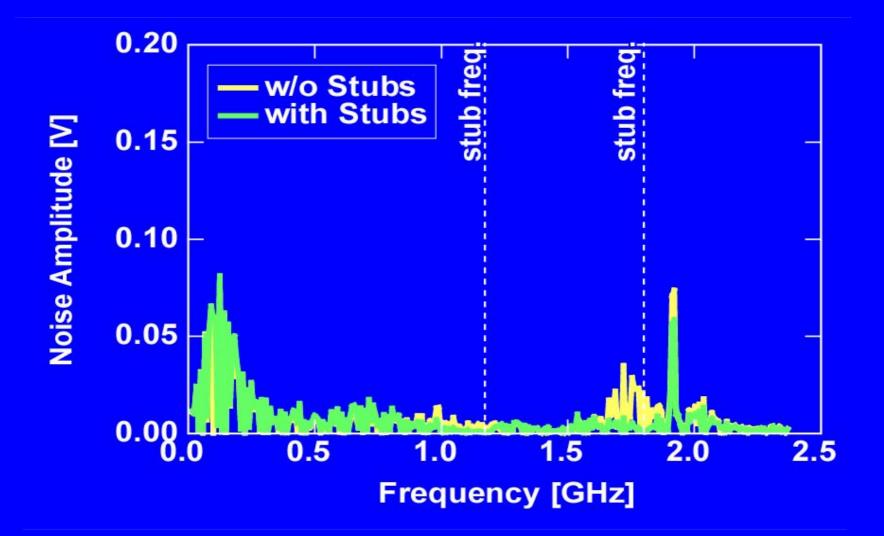
# Freq. Dependence @1.45GHz



# Freq. Dependence @1.80GHz

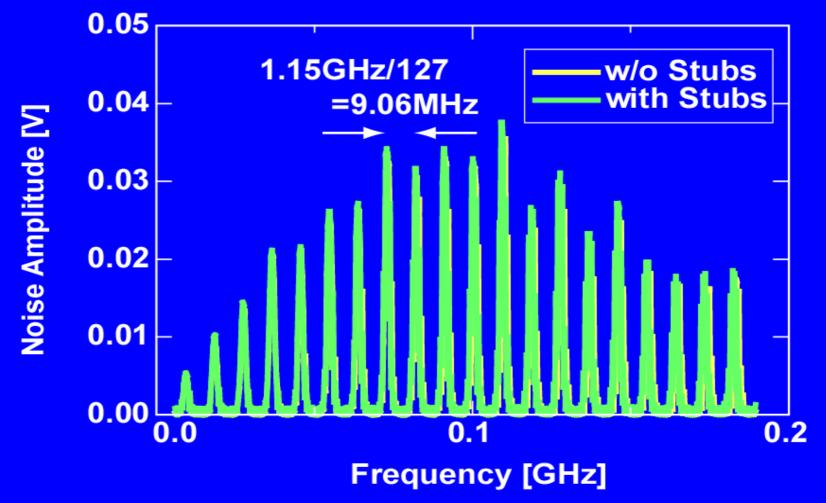


# Freq. Dependence @1.85GHz



## **Spectrum of Lower Frequency**

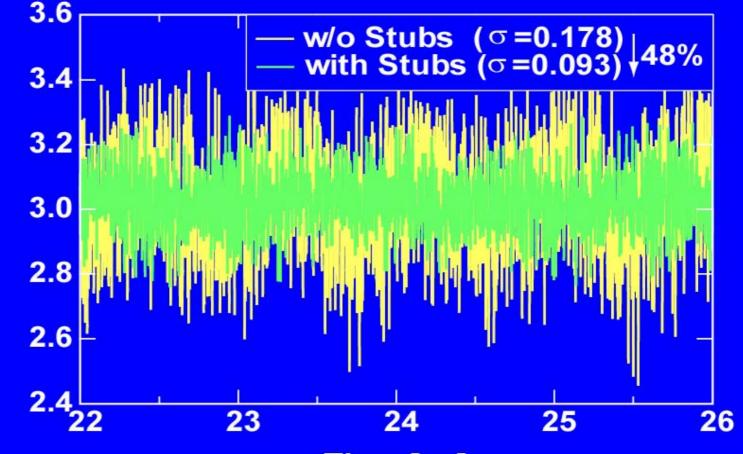
#### PRBS 2^7-1 characteristics



## Waveforms @1.15GHz Random

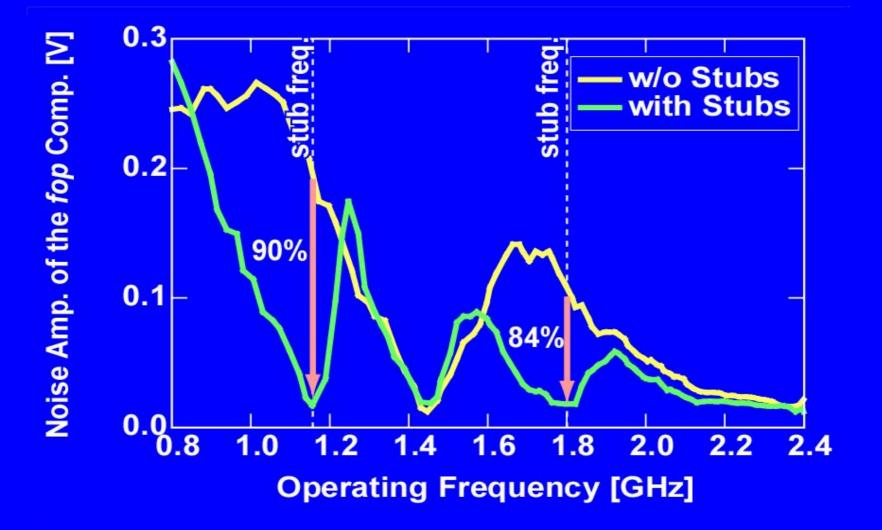
• Noise amplitude is evaluated by  $\sigma$ 

Voltage [V]



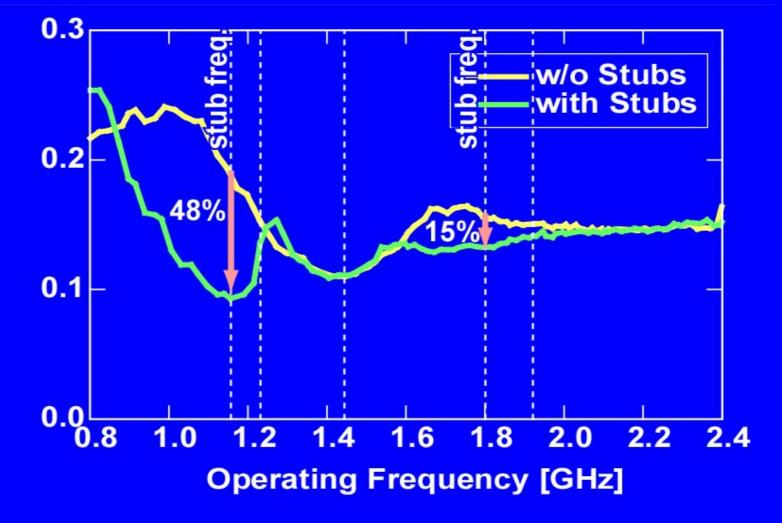
Time [ns]

## Noise of the fop Component



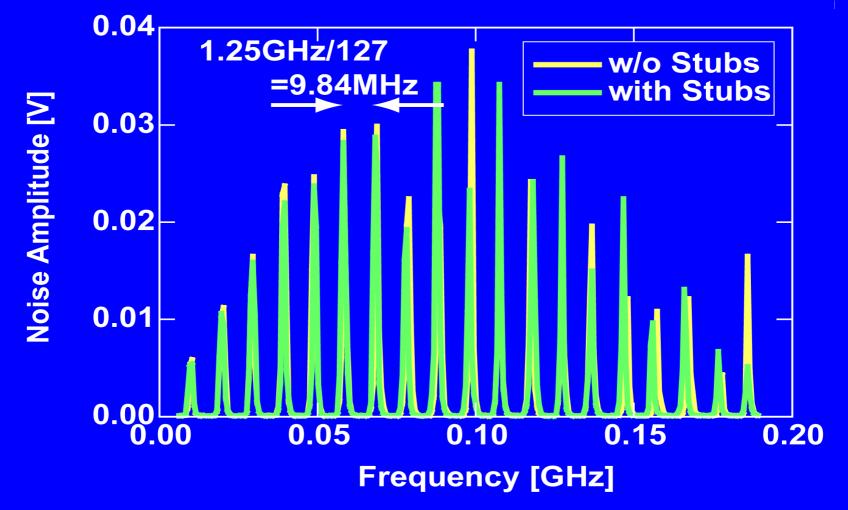
# Total Noise Amplitude ( $\sigma$ )

**Noise Amplitude (σ) [V]** 



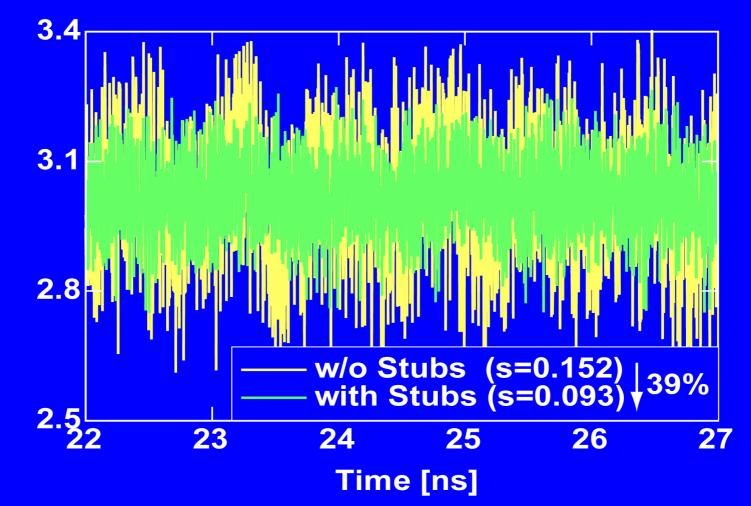
### **Spectrum of Lower Frequency**

#### PRBS 2^7-1 characteristics



## Waveforms @1.25GHz Random

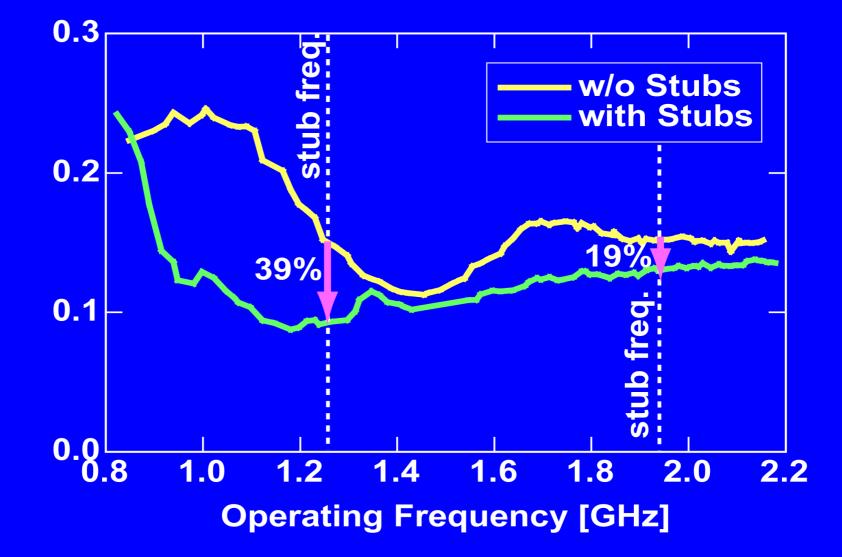
• Noise amplitude is evaluated by  $\sigma$ 



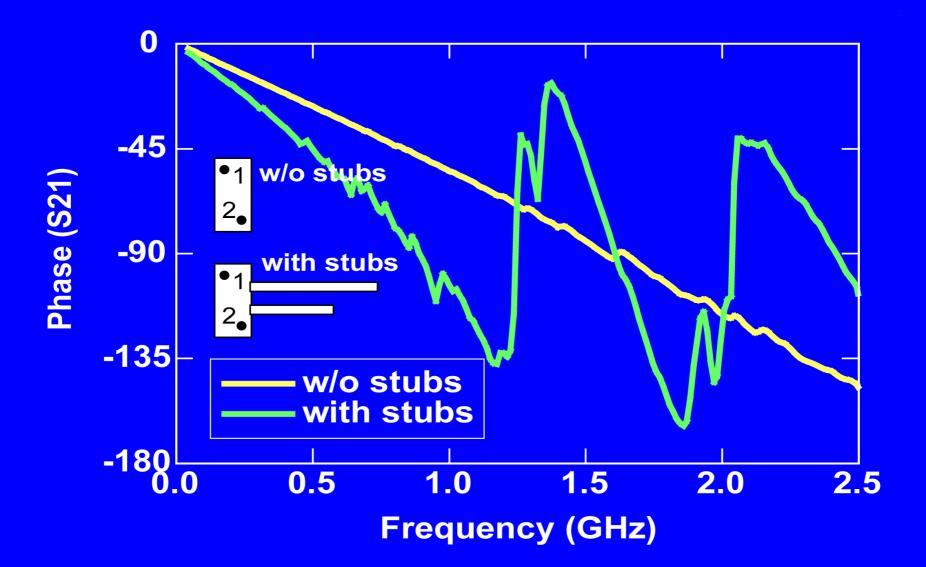
Voltage [V]

# Total Noise Amplitude ( $\sigma$ )

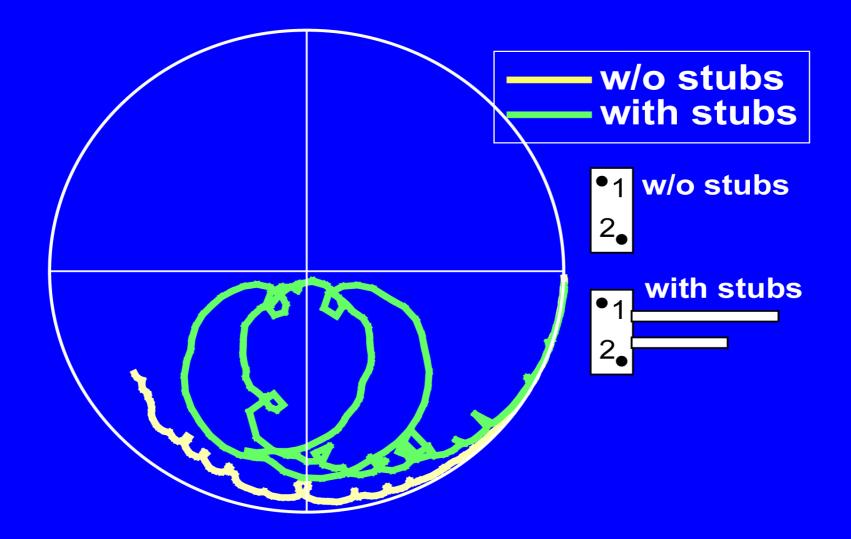




## S parameter – arg(S21)



## S parameter – S21



## **Short Summary**

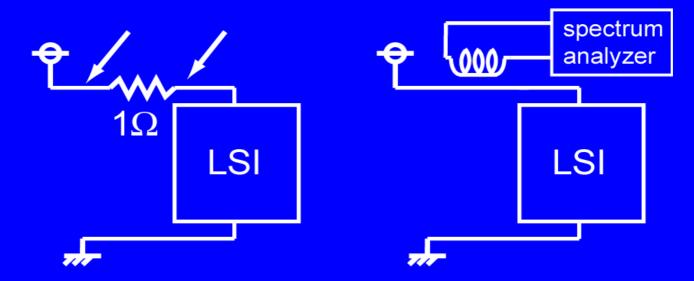
- The on-chip stub does not show the power supply reduction effects
  - Many bents, large resistance
- The off-chip stubs show clear noise reduction
  - 90% of the operating frequency component, 48% total noise is suppressed
  - Stub frequency dependence is observed
- Straight on-chip stub will be possible in the near future (~4mm@10GHz)

# **On-chip di/dt Detector**

### **Conventional Current Meas.**

- Probe the voltage difference of the R

   Needs numerical calculation
- Probe the magnetic field by pickup coil
   Phase information is lost

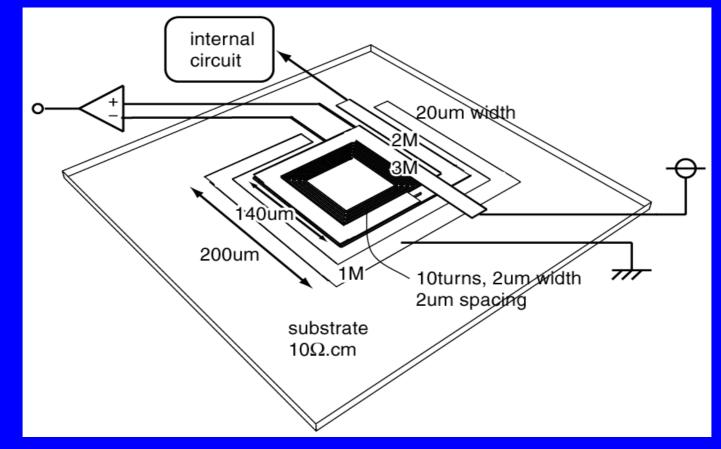


## Advantage

- On-chip
- di/dt waveform without numerical calculation
- Real time
- Feedback di/dt control is possible

## **Mutual Inductor**

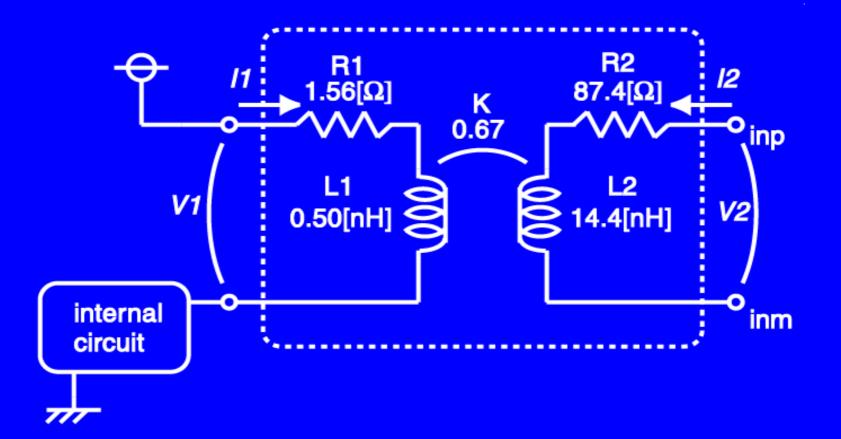
#### 0.35um, 3ML standard CMOS process



Large: 200um diameter, 24 turns

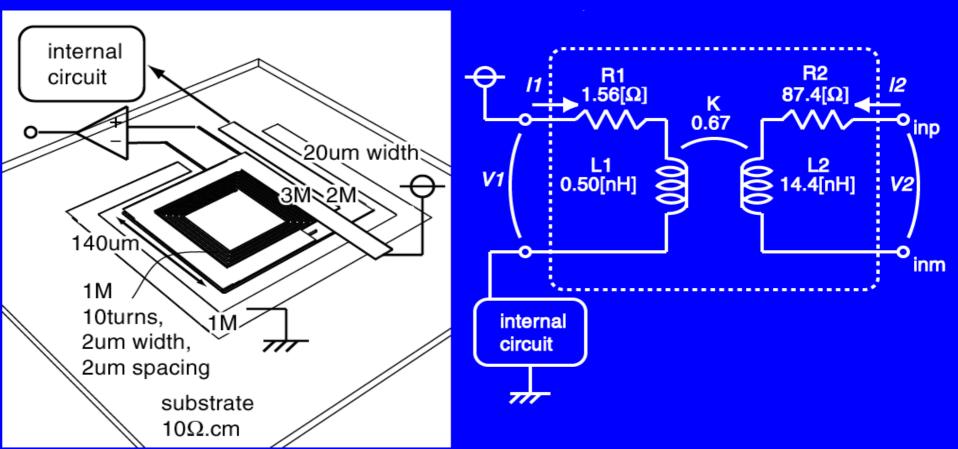
### **Equivalent Circuit**

#### Extracted by FastHenry

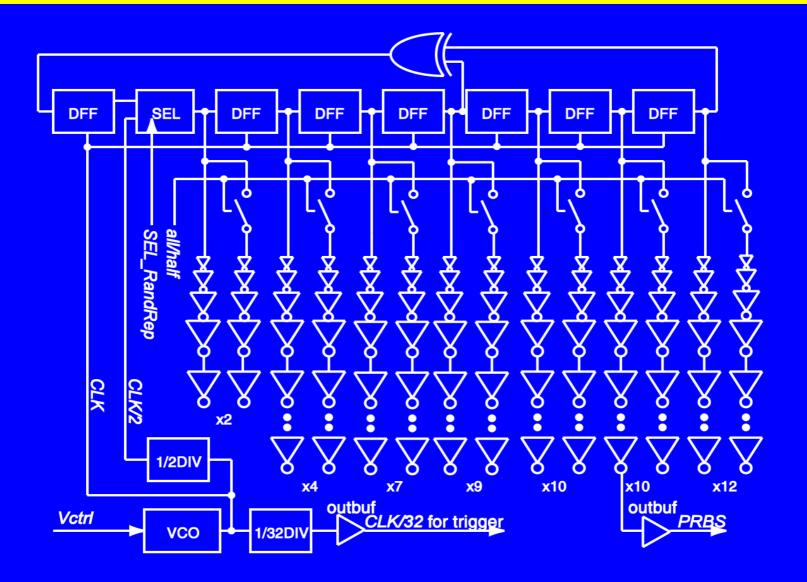


### **Mutual Inductor**

- 0.35um, 3ML standard CMOS process
- FastHenry extracts the equivalent circuit

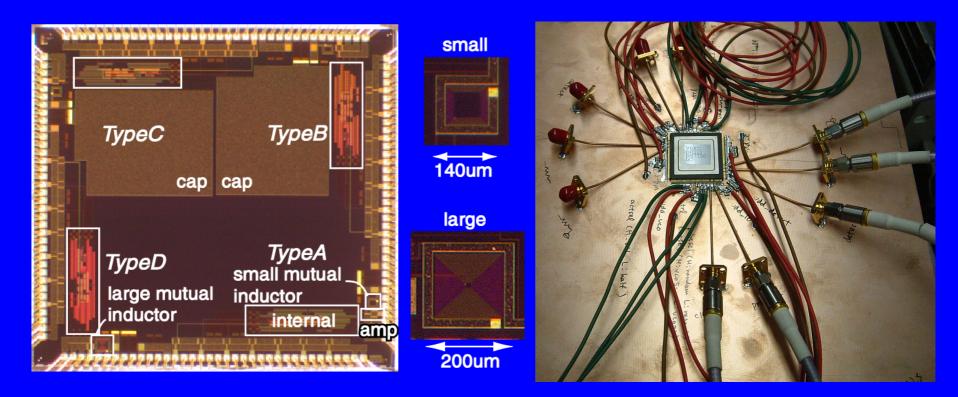


### **Internal Circuit as Noise Source**

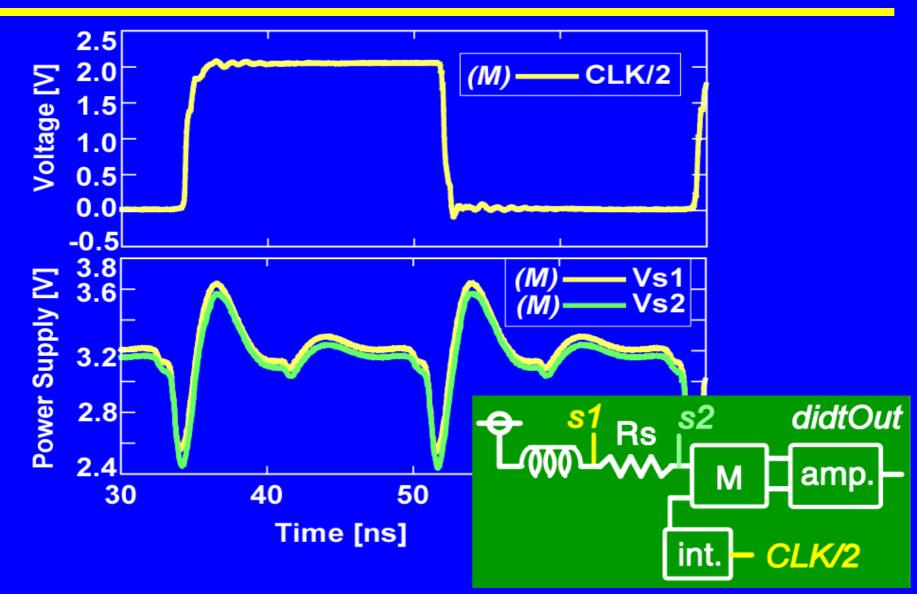


# **Chip Photograph**

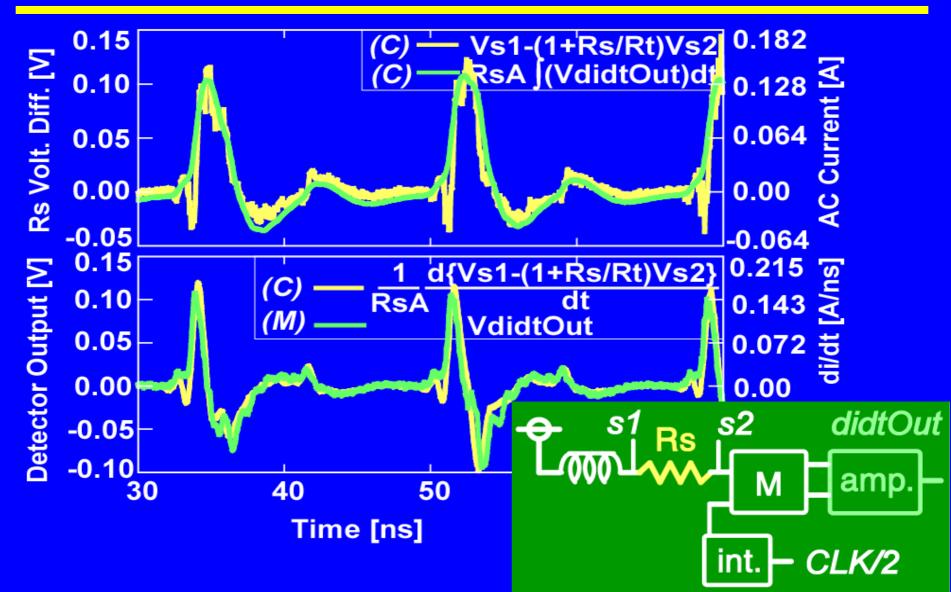
- 0.35um 3ML 2P CMOS (4.9mm x 4.9mm)
- The chip is mounted on a Cu board



#### Waveforms #1

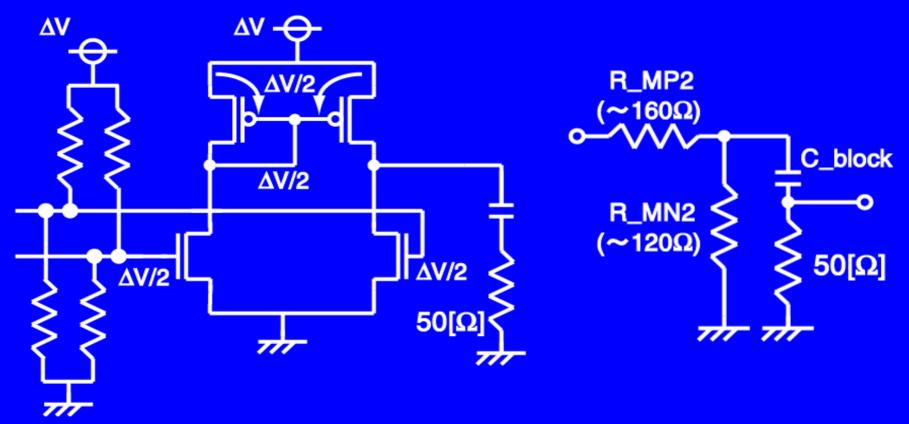


## Waveforms #2



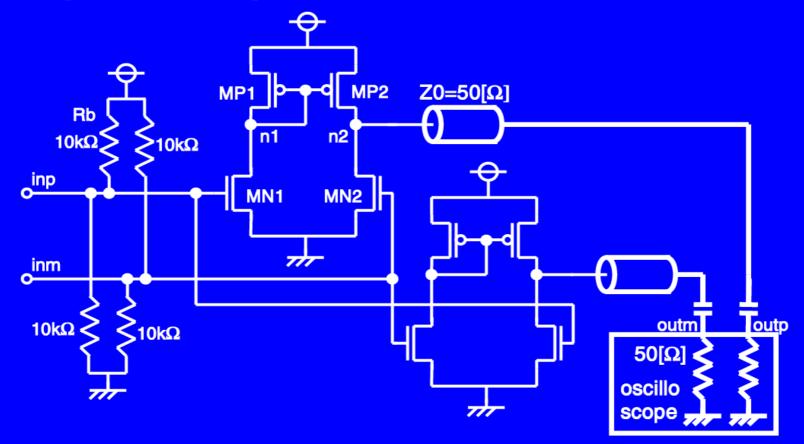
## **Noise Tolerance**

- Common mode noise is eliminated
- Vdd noise is suppressed to 18% (by 82%)



# Single or Dual?

- Noise immunity, Sensitivity, Symmetric
- Require two pins, numerical calculation



## Equations

$$V_{2} = K \sqrt{L_{1}L_{2}} \frac{dI_{1}}{dt} \qquad V_{s1} - \left(1 + \frac{R_{s}}{R_{t}}\right) V_{s2} = R_{s}I_{1}$$

$$V_{didtOut} = GV_{2} = GK \sqrt{L_{1}L_{2}} \frac{dI_{1}}{dt} \qquad V_{s1} - \left(1 + \frac{R_{s}}{R_{t}}\right) V_{s2} = R_{s}I_{1}$$

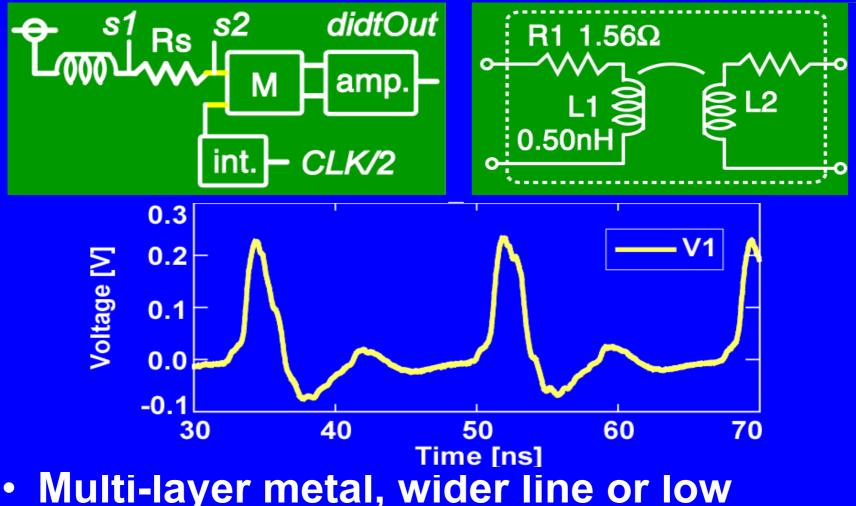
$$\frac{dI_{1}}{dt} = \frac{1}{GK \sqrt{L_{1}L_{2}}} V_{didtOut} = A_{v2didt} V_{didtOut}$$

$$\frac{dI_{1}}{dt} = \frac{1}{GK \sqrt{L_{1}L_{2}}} \qquad \frac{dI_{1}}{dt} = A_{v2didt} V_{amp_outRange_lin}$$

$$I_{1} = A_{v2didt} \int V_{didtOut} dt + C \qquad \frac{dI_{1}}{dt} = A_{v2didt} V_{didtOut_res}$$

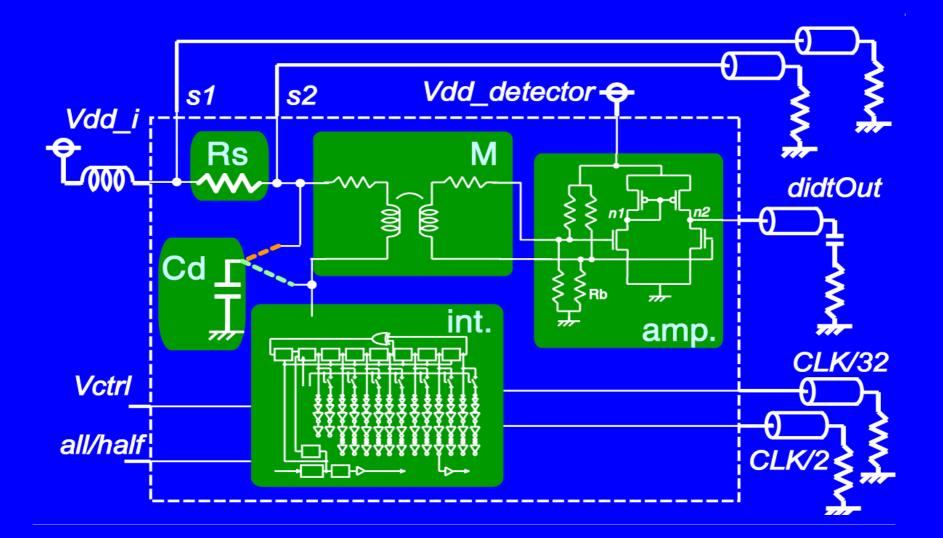
- L1=0.5nH, L2=14.4nH, K=0.67, G=0.385,
- Rs=0.78Ω, Rt=50Ω
- Vamp\_lin=±0.35V, di/dt\_range=±0.5x10<sup>9</sup>A/s

#### di/dt Detector Impedance

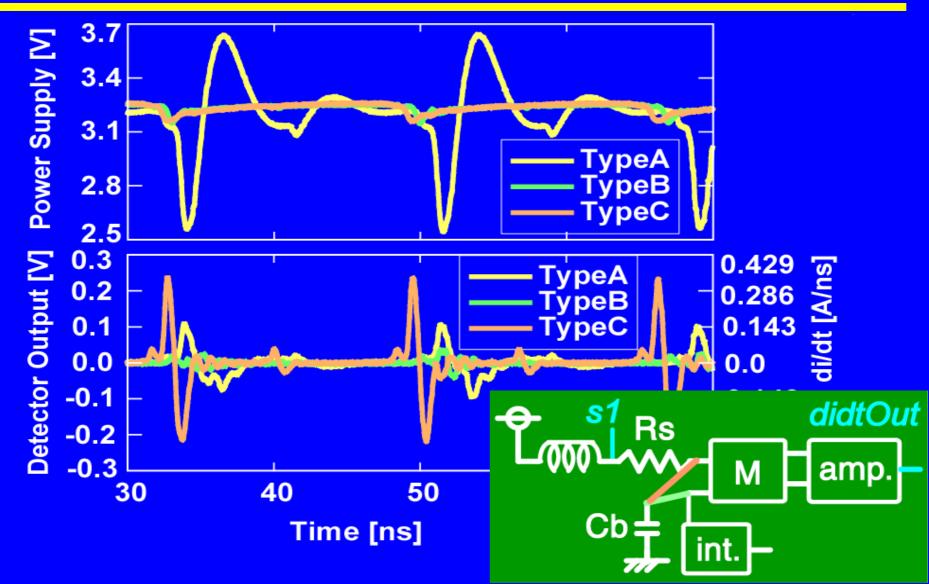


sensitivity can reduce the voltage drop

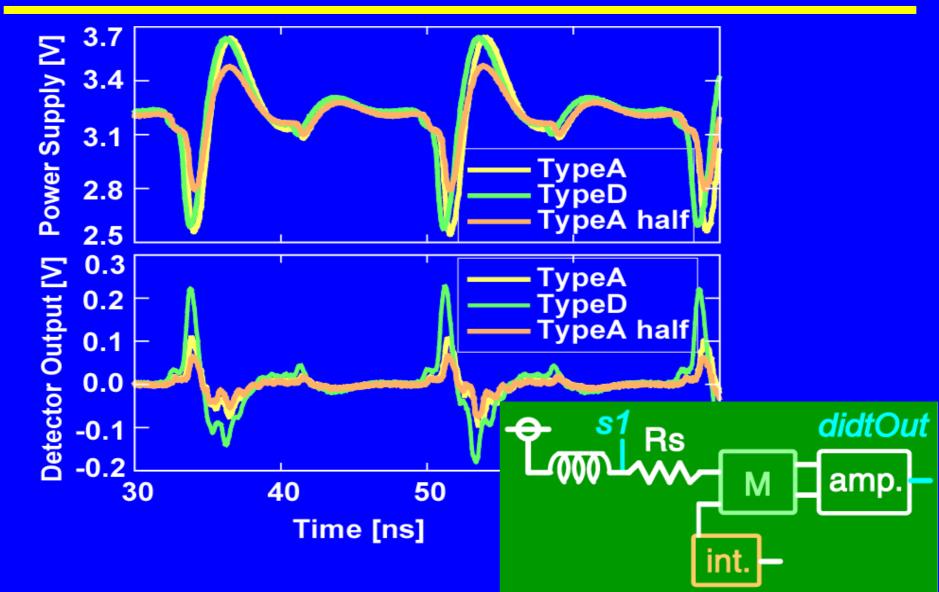
## Whole Circuit / Meas. Setup



## **Decoupling Capacitor Effects**

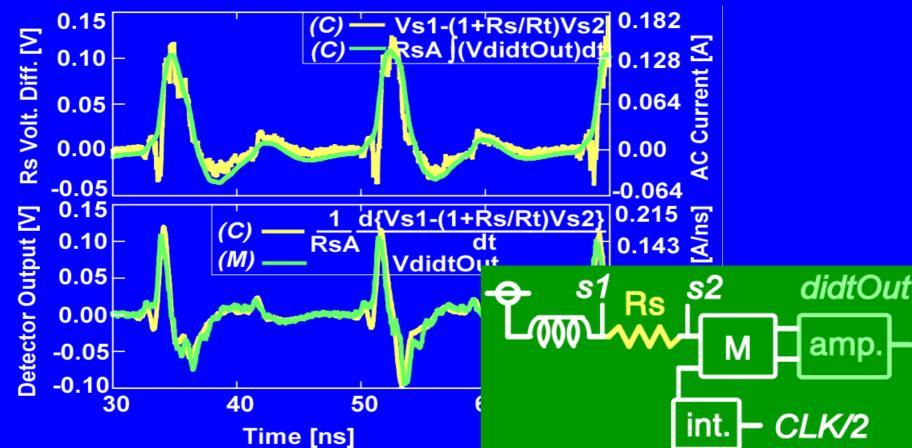


#### **Activation, M dependence**



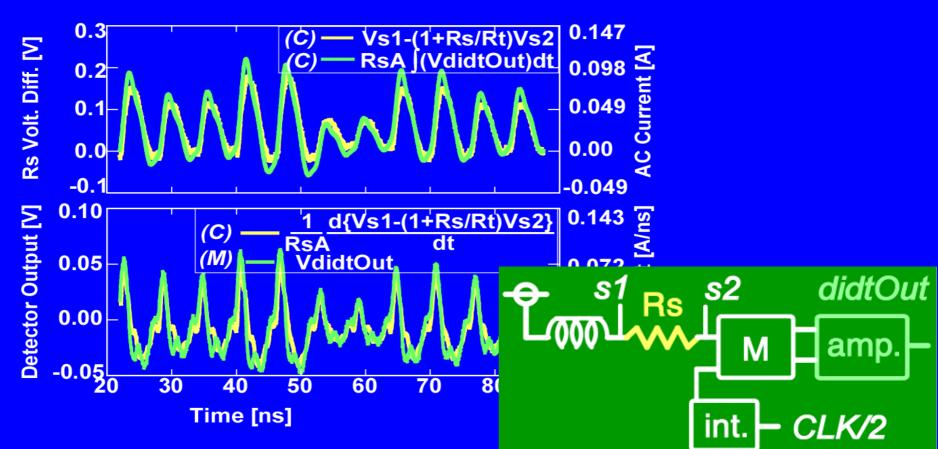
#### Error

- δ=4.49mV, I=5.8mA
- δ=4.38mV, dl/dt=6.3mA/ns

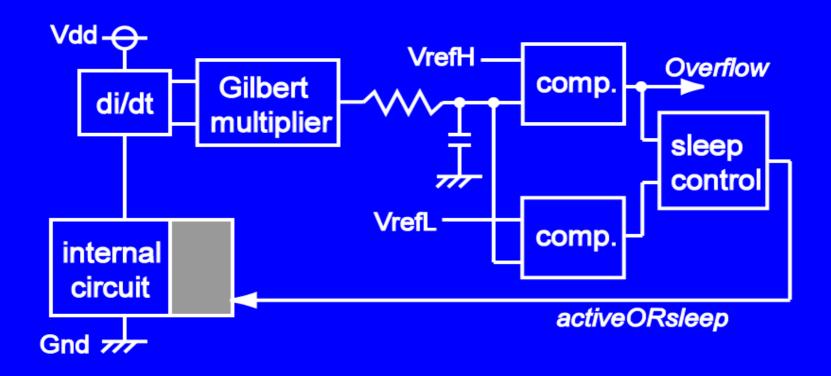


#### Error

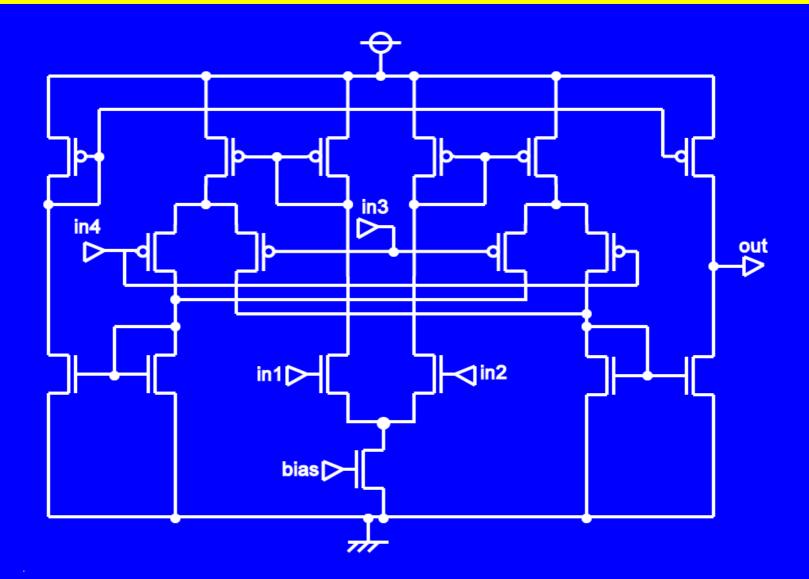
- σ=9.10mV, I=4.46mA
- σ=6.30mV, dl/dt=9.01mA/ns



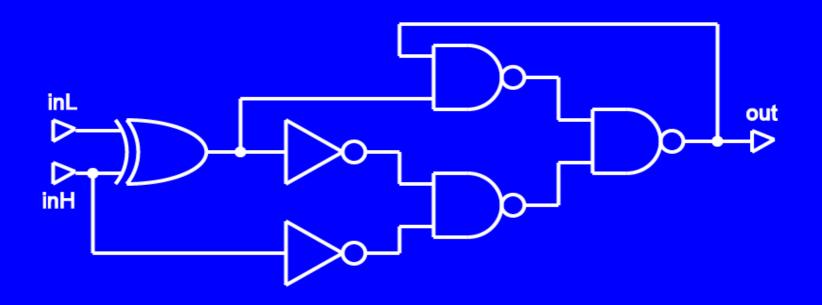
#### Feedback di/dt Control



## **Gilbert Multiplier**

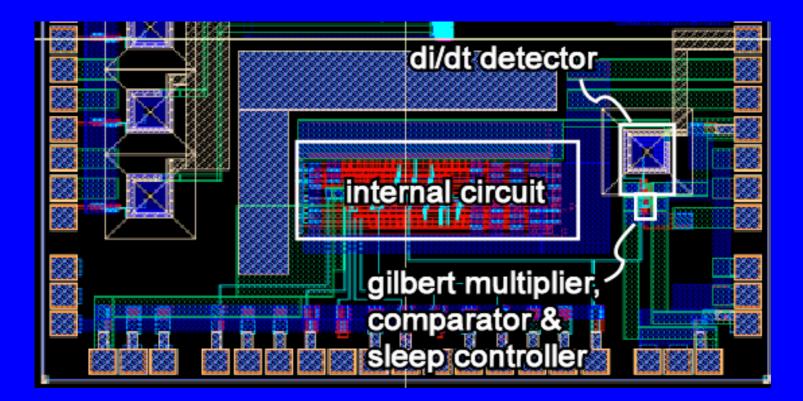


## **Sleep Controller**

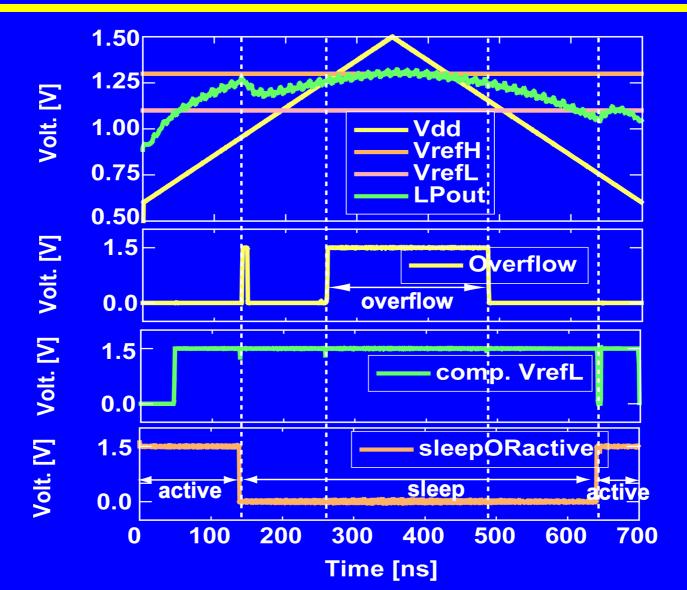


## **Chip Layout of di/dt Controller**

#### 0.15um SOI-CMOS technology



#### **Simulation Waveforms**

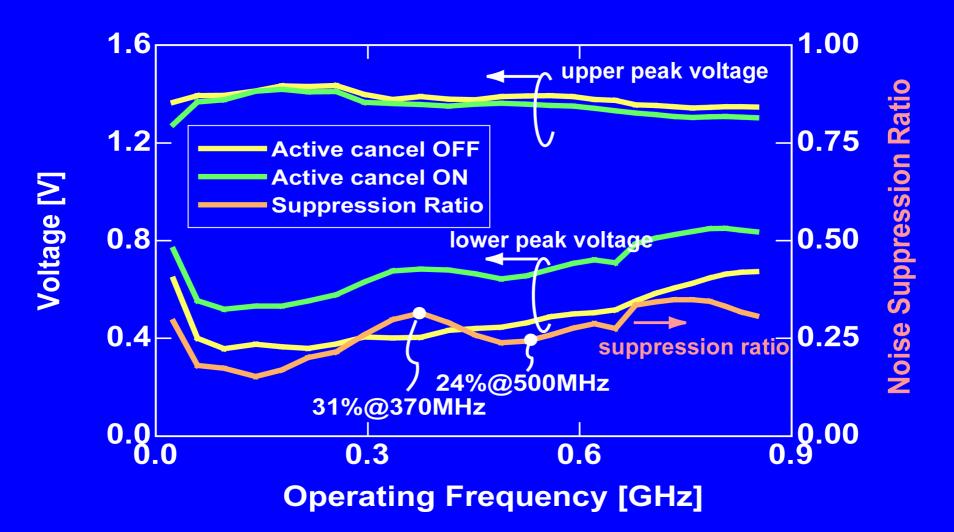


## **Short Summary**

- On-chip di/dt detector is demonstrated
- It consists of a power supply line, underlying spiral inductor, an amplifier
- di/dt waveforms obtained from the di/dt detector and the resistor agree well
- Current waveform can be calculated by integrating the detector output by time
- The di/dt detector circuit detects the decoupling capacitor effects as well

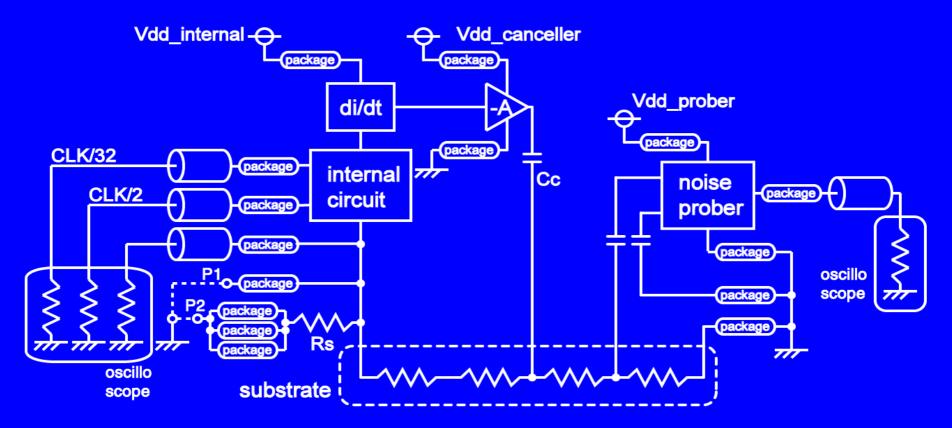
## **Active Noise Cancelling**

### Frequency Dependence (random)



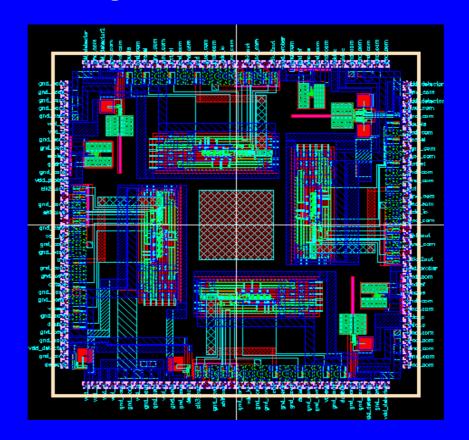
#### **Overall Circuit**

#### Change the Gnd line impedance by the chip mount

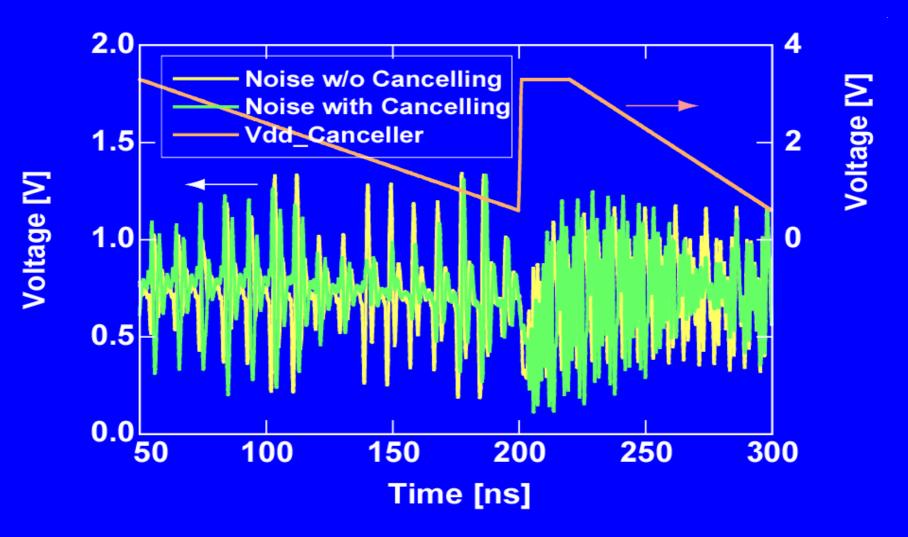


# **Chip Layout**

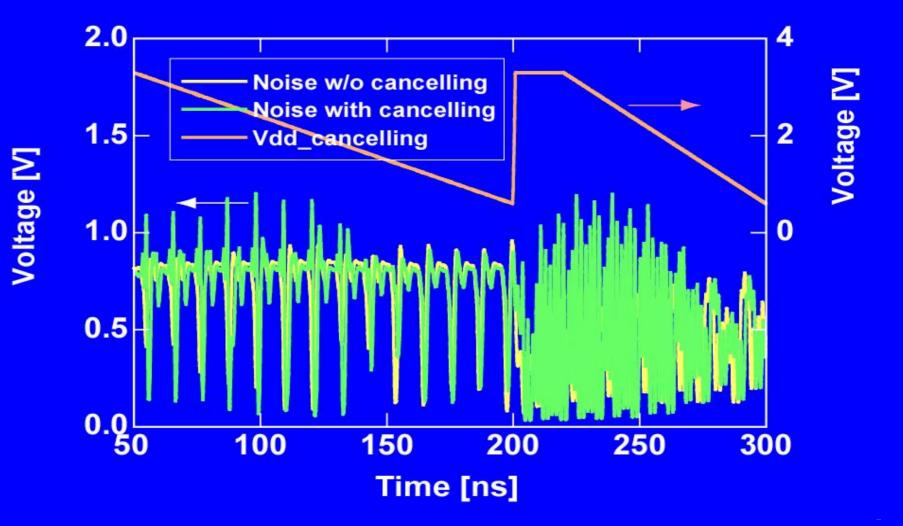
- 0.35um 3ML 2P CMOS (4.9mm x 4.9mm)
- Chip delivery date will be 10/8



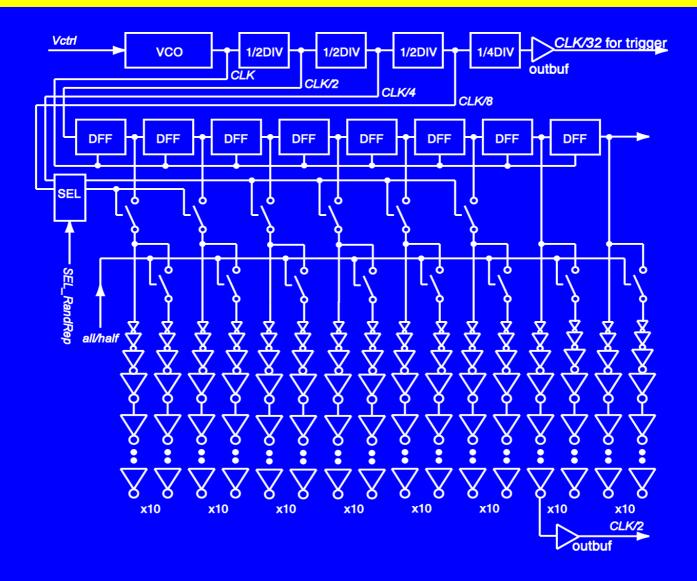
# Waveforms (Inductive)



# Waveforms (Resistive)



#### **Internal Circuit as Noise Source**



## **Future Works**

# **Conclusion (1/2)**

#### Chapter 2

- Stubs and decoupling capacitors are compared for power supply noise reduction
- Boundary frequency is clarified
- Circuit simulations confirmed the noise reduction
- Stubs will have more advantage over capacitors for LSIs with higher operating frequency
- Chapter 3
  - The on-chip stub does not show the power supply reduction effects because of bents, resistance
  - The off-chip stubs show clear noise reduction
  - Stub frequency dependence is observed
  - Straight on-chip stub integration will be possible in the near future

# Conclusion (2/2)

- Chapter 4
  - On-chip di/dt detector is demonstrated
  - di/dt waveforms obtained from the di/dt detector and the resistor agree well
  - Current waveform can be calculated by integrating the detector output by time
- Chapter 5
  - Feedforward active noise cancelling is proposed
  - di/dt is used for anti-phase signal generation, and injected into substrate
  - No-body-contact amplifier is used for the probing
  - Simulation results show the substrate noise cancelling effects for a test circuit