



SMART ACCESS IMAGE SENSORS FOR HIGH-SPEED AND HIGH-RESOLUTION 3-D MEASUREMENT BASED ON LIGHT-SECTION METHOD

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ABSTRACT—This contribution is devoted to high-speed and high-resolution 3-D imaging based on the light-section method. Our smart access image sensors achieve high-speed position detection on the sensor plane to realize real-time 3-D imaging with high range accuracy. A high-speed position sensor using a quad-tree scan implementation achieves 10k points/s position detection of a projected spot beam. To reduce the number of frames required for a 3-D image, we present high-speed position sensors with new row-parallel architectures to get positions of a projected sheet beam efficiently. Moreover we present a high-speed readout scheme with adaptive threshold circuits to realize a higher-resolution 3-D image sensor employing a compact pixel circuit. We discuss the features and advantages of smart access methods for advanced 3-D imaging applications on the basis of comparison.

Key Words: Smart Access, CMOS Image Sensor, Position Sensor, Real Time, High Resolution, 3-D Measurement, Light-Section Method

1. INTRODUCTION

3-D measurement system has a wide variety of application fields such as robot vision, computer vision and position adjustment. In recent years we often see 3-D computer graphics in movies and televisions, and handle them interactively using personal computers and video game machines. Then 3-D imaging systems will be applied to scene segmentation without a chroma-key system, gesture recognition, advanced security systems and so on. Latest and future 3-D applications will require both highly accurate and real-time range finding.

Some range finding methods were proposed for 3-D measurement, for example, the stereo-matching method, the time-of-flight (TOF) method [1]–[8] and the light-section method [9]–[12]. These typical methods have been used for various applications selectively because of their drawbacks and advantages. The stereo-matching method provides a simple system configuration with two or more cameras, in other words, it provides a passive imaging system. Therefore it can be applied to various measurement environments and target objects in simple way. On the other hand, the stereo-matching processing requires huge computational effort for high-resolution range finding. And the range accuracy is practically limited by an ambient light and a target surface pattern. Thus the stereo-matching method is suitable for a kind of shape recording under ideal measurement situations, or a gesture recognition system with rough range accuracy. The TOF method is another typical range finding method. A projected light is reflected from a target object with some delay proportional to the distance. A camera detects the arrival time of the reflected light to measure the distance. The absolute range resolution is determined by the time resolution of incident light detection. The range accuracy is constant independently of the target distance, however, it is limited at a couple of centimeter by the electronic shutter speed. Therefore the TOF method is being applied to long-range 3-D measurement such as shape measurement of buildings and monuments.

The light-section method is most suitable for a middle-range 3-D measurement system with high range resolution. It has the capability of < 1mm range finding at a distance of several meters, and high robustness of measurement environment due to active range finding. These features are required especially for 3-D pictures and movies in the real world, advanced gesture recognition systems detecting slight finger

motions, accurate shape measurement for custom-made wares, and various scientific observation. These future applications, however, need a real-time 3-D measurement system, and it is difficult for a standard imaging system since a very high-speed frame rate is necessary to reconstruct a range map. A range map requires a lot of position detections during beam scanning. For example, a range map with 1M pixels (1024×1024 pixels) requires 1M position detections per range map in a 3-D measurement system using a spot beam X-Y scanner. Thus 30M fps position detection is necessary for 30 range maps/s range finding with 1M pixels. A 3-D measurement system with a sheet beam scanner can reduce the number of frames for a range map, nevertheless 30k fps position detection is needed to realize a real-time range finding system. Even the high-speed CMOS image sensors with parallel ADCs realize 500 – 2000 fps at most [13]–[14]. Therefore an efficient access method is necessary for a real-time and high-resolution 3-D imaging system based on the light-section method.

Some high-speed position sensors have been reported in [10]–[11] and [15]–[17]. The conventional position sensors [15]–[17] have been developed especially for high-speed range finding based on the light-section method. The sensor using a row-parallel winner-take-all (WTA) circuit [15] can acquire a 64×64 range map in 100 range maps/s. The pixel resolution, however, is limited by the precision of the current-mode WTA circuit. Therefore it is difficult to realize enough high frame rate for real-time range finding with high pixel resolution. The sensor using pixel-parallel architecture [16] achieves 192×124 range finding in video rate. It has a pixel large circuit for frame memories and an ADC. To reduce the pixel size, they developed a 320×240 (QVGA) color imager with analog frame memories out of the pixel array [17]. It makes a pixel circuit smaller and realizes 160×120 3-D imaging in 15 range maps/s, but the range finding rate is inferior to their previous work [16]. Therefore it is also difficult to get a 3-D image in real time with higher pixel resolution.

In Section 2, we present concepts of smart access to realize high-speed and high-resolution range finding. In Section 3, a high-speed position sensor using quad-tree scan is introduced, which has the capability of 10k points/s position detection of a projected spot beam. Three position sensors for a high-speed range finding system with sheet beam projection are shown in Section 4. Two row-parallel architectures for quick position detection on the sensor plane are proposed in Section 4.2 and Section 4.3. And then a real-time 3-D image sensor with high pixel resolution is presented in Section 4.4. It employs a high-speed readout scheme with adaptive threshold circuits, which allows a compact pixel circuit implementation for over-VGA pixel resolution. The performance comparison of these smart access image sensors is shown in Section 4.5. Finally Section 5 concludes the paper.

2 CONCEPTS OF SMART ACCESS FOR HIGH-SPEED POSITION DETECTION

Figure 1 (a) shows a raster scan method employed for standard CCDs and CMOS sensors. In the raster scan method, all the pixel values are read out just for a few activated pixels on the sensor plane. That is, it requires $O(N \times N)$ cycles for $N \times N$ pixel resolution so that it is not suitable for a high-speed 3-D measurement system. We propose smart access image sensors for high-speed position detection to realize fast range finding with high pixel resolution.

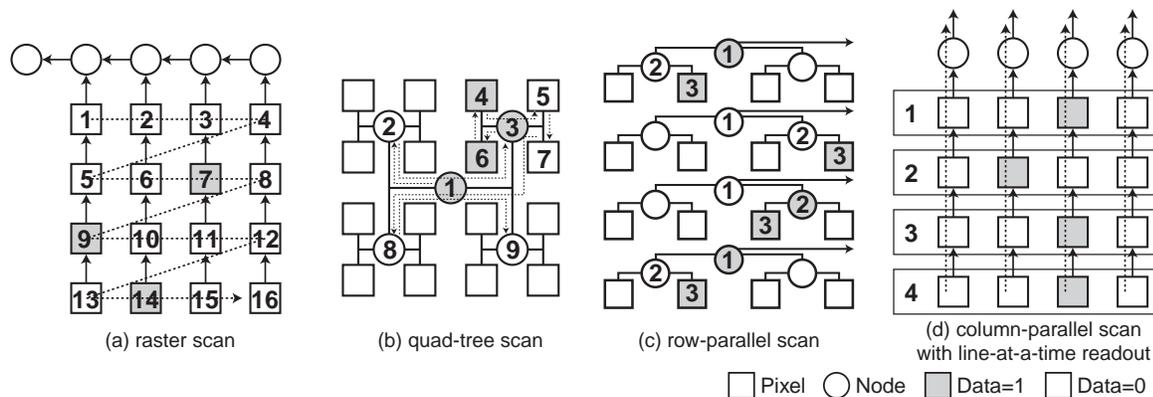


Figure 1. Access methods for activated pixel detection.

Figure 1 (b) shows a quad-tree scan method for quick position detection [18]. It can reduce the number of cycles for position detection efficiently when activated pixels exist locally on the sensor plane. The operation cycles are $O(\log_2 N)$ theoretically. It is suitable for position detection of a projected spot beam since it is effective for a few activated pixels on the sensor plane. We present a novel implementation of quad-tree scan on the sensor plane and show a developed position sensor with 256×256 pixel resolution in Section 3.2.

Figure 1 (c) shows a row-parallel architecture for high-speed activated pixel search [19]–[21]. It is suitable for a range finding system with sheet beam projection since it is efficient to detect localized activated pixels in each row. Our search algorithms achieve high frame rate of position detection with compact circuit implementation. In Section 4.2, we introduce a row-parallel search architecture using a chained search circuit and a bit-streamed column address flow. These techniques are implemented on the sensor plane. In Section 4.3, another row-parallel search architecture is presented. It utilizes a novel implementation of row-parallel binary-tree scan. These smart access methods and circuit implementations have the capability of around 1000 range maps/s for a future high-speed 3-D camera.

Figure 1 (d) shows a column-parallel scan method with line-at-a-time readout, which has high-speed position detectors in column parallel and achieves $O(N)$ cycles for activated pixel detection. The number of required cycles is larger than the row-parallel scan method, but it has a possibility of higher pixel resolution in real-time range finding due to compact pixel circuits. Our high-speed readout scheme with adaptive threshold circuits achieves 30 – 60 range maps/s in over-VGA pixel resolution [22]–[23]. It is suitable for a real-time range finding system with higher image/range resolution.

3 SMART ACCESS IMAGE SENSOR FOR SPOT-BEAM-PROJECTION SYSTEM

3.1 Principle of 3-D Measurement with Spot Beam Projection

In a 3-D measurement system with spot beam projection, a projected spot beam is reflected on a target object and reached on the sensor plane. The range data of a target object are acquired by triangulation with the projected beam direction and the position of incident beam on the sensor plane.

Figure 2 shows a principle of triangulation-based range calculation. A light source and a camera are placed at a distance of d as shown in Figure 2. It means a parallax of triangulation. And then a scanning mirror provides α_1 and θ as a direction of projected beam. θ can be also provided from the Y position of projected beam on the sensor plane. When a target object is placed at $p(x_p, y_p, z_p)$, a position sensor detects the reflected beam at $e(x_e, y_e)$ in Figure 2. α_2 and θ are given by

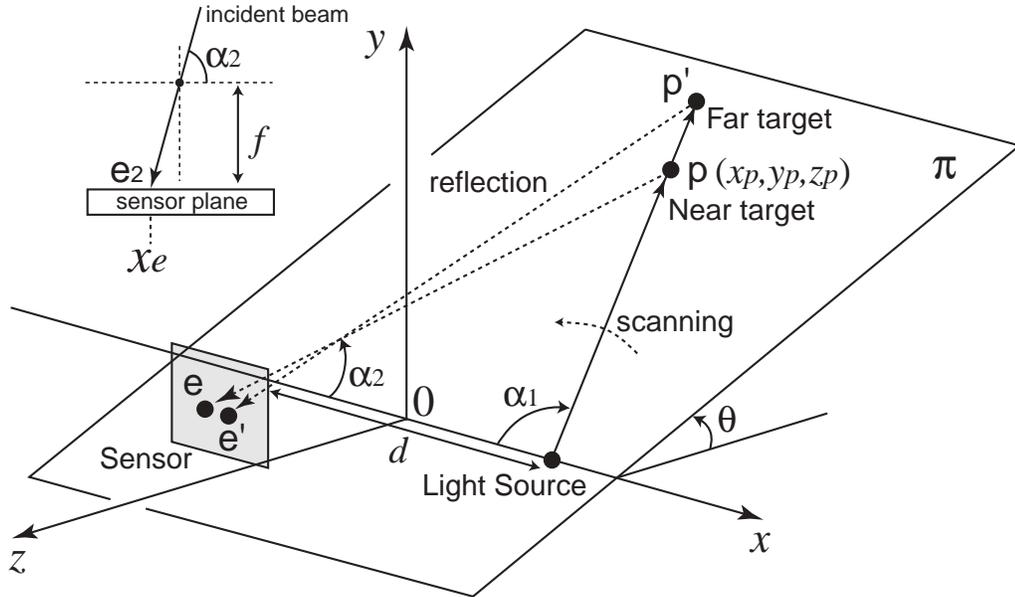


Figure 2. Principle of triangulation-based range calculation.

$$\tan \alpha_2 = \frac{f}{x_e} \quad (1)$$

$$\tan \theta = \frac{f}{y_e} \quad (2)$$

where f is a focal depth of a camera. α_1 and α_2 are also represented by

$$\tan \alpha_1 = \frac{l}{d/2 - x_p} \quad (3)$$

$$\tan \alpha_2 = \frac{l}{d/2 + x_p} \quad (4)$$

where l is length of a perpendicular line from p to X-axis. Therefore x_p and l are given by

$$x_p = \frac{d(\tan \alpha_1 - \tan \alpha_2)}{2(\tan \alpha_1 + \tan \alpha_2)} \quad (5)$$

$$l = \frac{d \tan \alpha_1 \tan \alpha_2}{\tan \alpha_1 + \tan \alpha_2} \quad (6)$$

Here $y_p = l \sin \theta$ and $z_p = -l \cos \theta$.

$$y_p = \frac{d \tan \alpha_1 \tan \alpha_2 \sin \theta}{\tan \alpha_1 + \tan \alpha_2} \quad (7)$$

$$z_p = -\frac{d \tan \alpha_1 \tan \alpha_2 \cos \theta}{\tan \alpha_1 + \tan \alpha_2} \quad (8)$$

A range image of a target scene can be acquired by the range calculation using whole position detections of a scanning beam.

3.2 High-Speed Position Sensor Using Quad-Tree Scan

3.2.1 Concept of Quad-Tree Scan

Figure 3 shows the concept of quad-tree scan, which reduces redundant cycles in scanning images for position detection of a projected spot beam. The value of a node in a quad-tree is the logical-OR of all pixels included in its lower level. For example, the value of the node at the top of the quad-tree in Figure 3 is the logical-OR of 4×4 pixels. The value of a node in the second level (level 1 in Figure 3) is the logical-OR of 2×2 pixels.

Figure 4 shows an example of the quad-tree scan sequence. At the beginning of quad-tree scan, the node at the top of the quad-tree is scanned. In Figure 4 (a), the value of the node is 1, so the node at its lower level is scanned in the next step. In Figure 4 (b), the value of the node is 0, so the scan of nodes at its lower level is skipped in the next step. If the scan of all four nodes in a level is finished, the node at upper level is scanned in the next step (ex. Figure 4 (g)–(h)). In the case of Figure 4, the number of cycles needed to scan the entire image is 9. In raster scan, the number of cycles needed to scan the same image is 16. We can reduce redundant cycles in scanning images using quad-tree scan in comparison with raster scan. In higher resolution, the trend becomes more significantly.

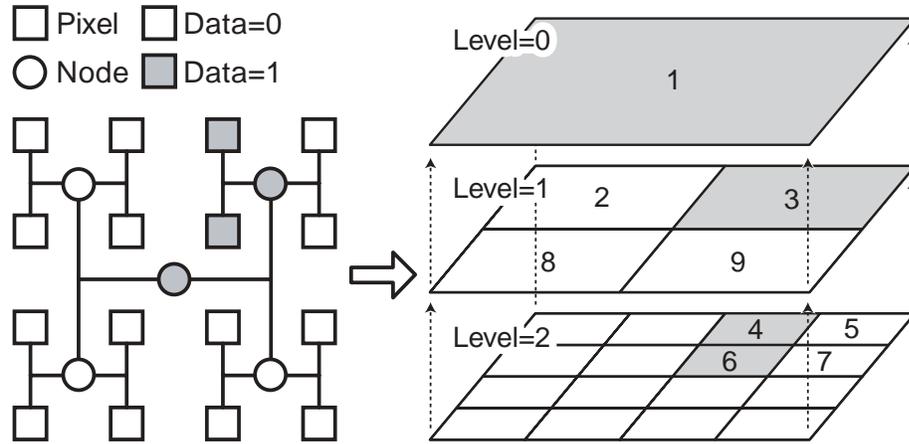


Figure 3. Concept of quad-tree scan method.

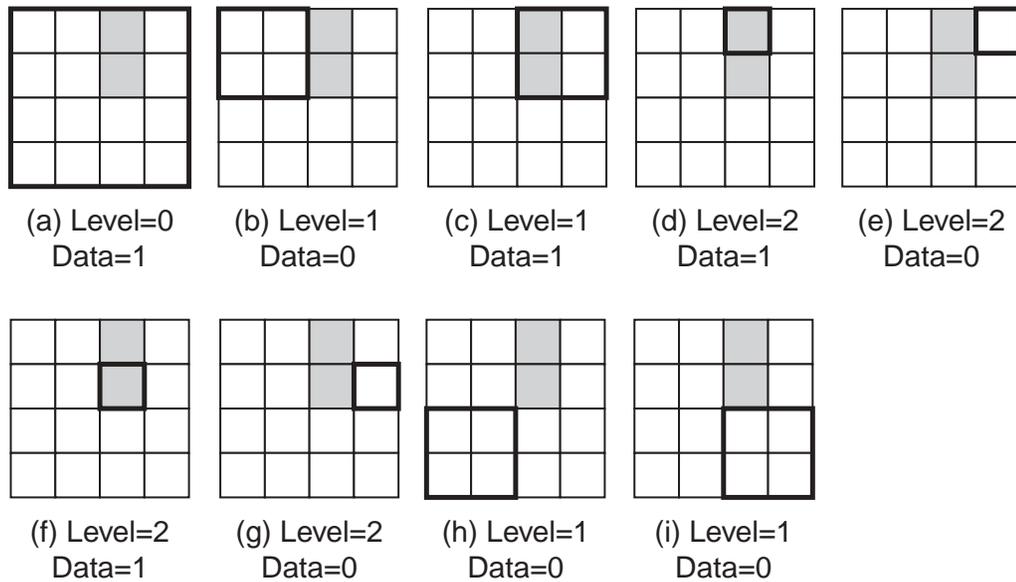


Figure 4. Sequence of quad-tree scan.

3.2.2 Circuit Realization

Figure 5 shows a schematic of a pixel. A pixel is composed of a photo detector, a 1-bit D-latch and an output circuit. A photo detector is composed of a photo diode and a reset transistor. The reset transistor resets the output voltage of the photo detector. When the reset transistor turns off, the integration of the photo current begins. After integration phase, the D-latch converts the output voltage of the photo detector to a binary value. The output node of the D-latch is connected to the output circuit. The output circuit is a part of a dynamic logical-OR circuit.

The logical-OR of pixel values in a variable block is needed to realize the quad-tree scan mentioned in the previous section. Figure 5 also shows a schematic of a variable block logical-OR circuit. The variable block logical-OR circuit is composed of a row logical-OR circuit and column logical-OR circuits. A column logical-OR circuit is composed of a transistor for precharge and pull-down transistors included in all pixels as output circuits. A column logical-OR circuit calculates the logical-OR of pixel values in a column. The row logical-OR circuit calculates the logical-OR of output values of selected column logical-OR circuits.

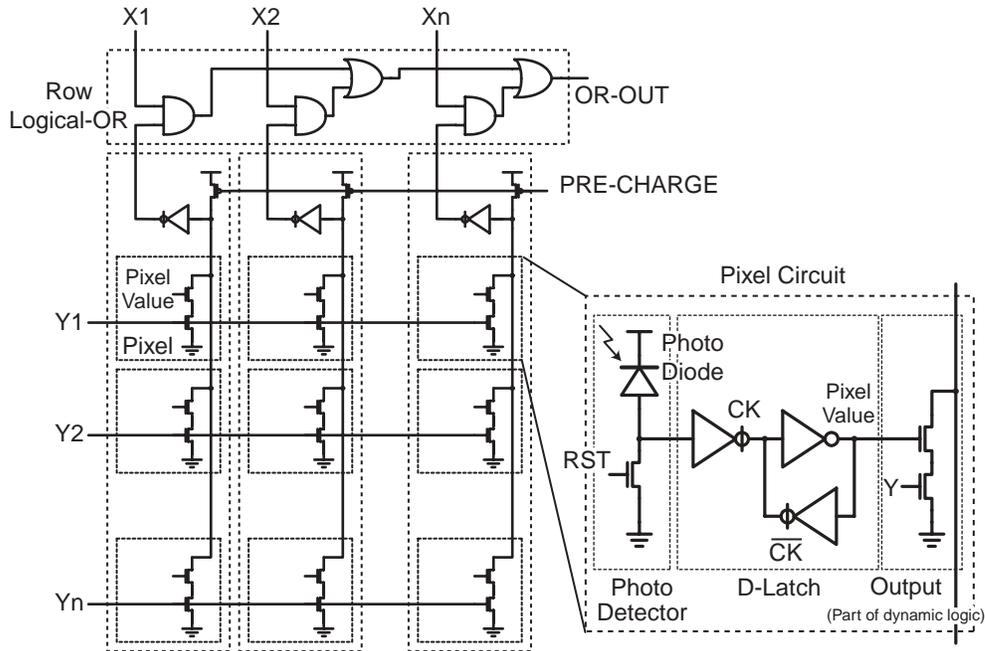


Figure 5. Schematic of a variable block logical-OR circuit and a pixel circuit.

Figure 6 shows a block diagram of a variable block address decoder. The address decoder for a variable block logical-OR circuit is composed of two standard address decoders and an address selector. The variable block address decoder activates address lines of the variable block logical-OR circuit between two addresses.

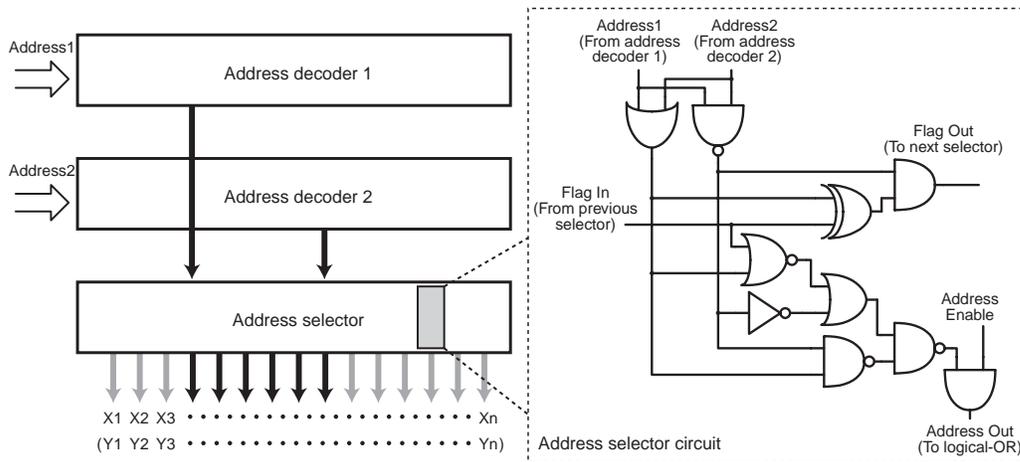


Figure 6. Variable block address decoder.

3.2.3 Chip Implementation

Figure 7 shows a microphotograph of the position sensor, and Table I shows parameters of the sensor. The sensor has a 256×256 pixel array, a set of address decoders and a variable logical-OR circuit on an 8.9 mm×8.9 mm die. The sensor is designed and fabricated in 0.6 μm CMOS 3-Metal 2-Poly-Si process.

3.2.4 Measurement Results

The 3-D measurement system is composed of the fabricated position sensor, a He-Ne laser source with an X-Y scanning mirror, and a personal computer (PC) with an ADC/DAC board and digital I/O boards.

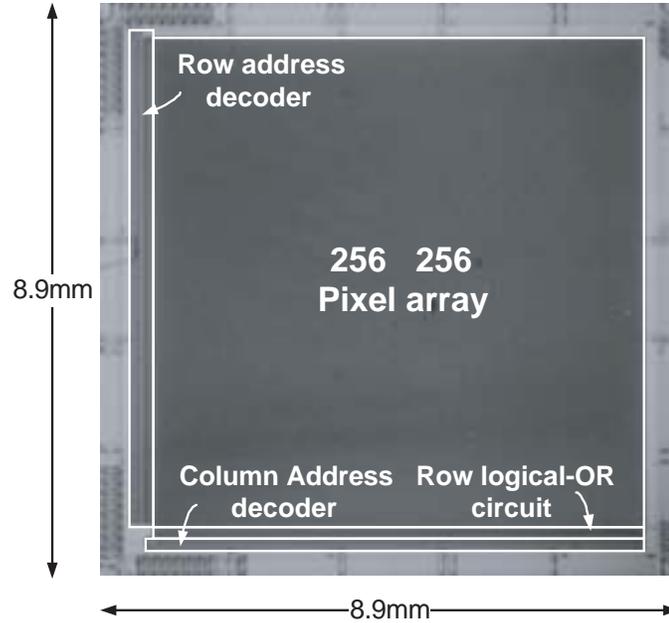


Figure 7. Microphotograph of the quad-tree scan sensor.

Table I. Specifications of the sensor.

Process	0.6 μm CMOS 3-metal 2-poly-Si
Die size	8.9 mm \times 8.9 mm
# of pixels	256 \times 256 pixels
Pixel size	28.0 μm \times 28.0 μm
Fill factor	22.1 %
# of FETs/pixel	13 transistors

The PC acquires image data through the digital I/O board and controls the sensor and the mirrors. In addition, the PC calculates the center of gravity of the laser spot.

Figure 8 (a) shows an acquired image of a laser spot. The integration time of photo current is 100 μs . The number of activated pixels is 1 – 8. The number of cycles needed for quad-tree scan is 30 – 90. The pixel activated by the effect of noise is not observed. In Figure 8 (b), 3-D positions of 100 \times 100 points are measured for a sphere target object. To evaluate the range accuracy, we measured a flat panel at a distance of 1265 mm from the focal point. The average error of measured range is 2.35 mm and the accuracy is 0.19 % when the 3-D positions of 8 \times 8 points in a 200 mm \times 200 mm area are measured. The error of X-Y position is 0.8 mm, which corresponds to 0.4 % accuracy.

The speed of 3-D measurement is 2500 points/s using a 2 MHz digital I/O board. In the circuit simulation, the sensor can work up to the speed of 10k points/s with higher-speed digital I/O board for sensor control.

3.2.5 Summary

Our quad-tree scan position sensor with 256 \times 256 pixels has been designed in 0.6 μm CMOS process and successfully tested. The sensor can detect the position of a laser spot quickly using implemented quad-tree scan. The quad-tree scan method is efficient for a few activated pixels in large pixel array. The center of gravity of a laser spot is calculated in the accuracy of sub-pixel level. The range accuracy is 0.4 % and the 3-D measurement speed is up to 10k points/s. The high-speed position detection can be applied to not only a 3-D measurement system but also tracking and position adjustment applications.

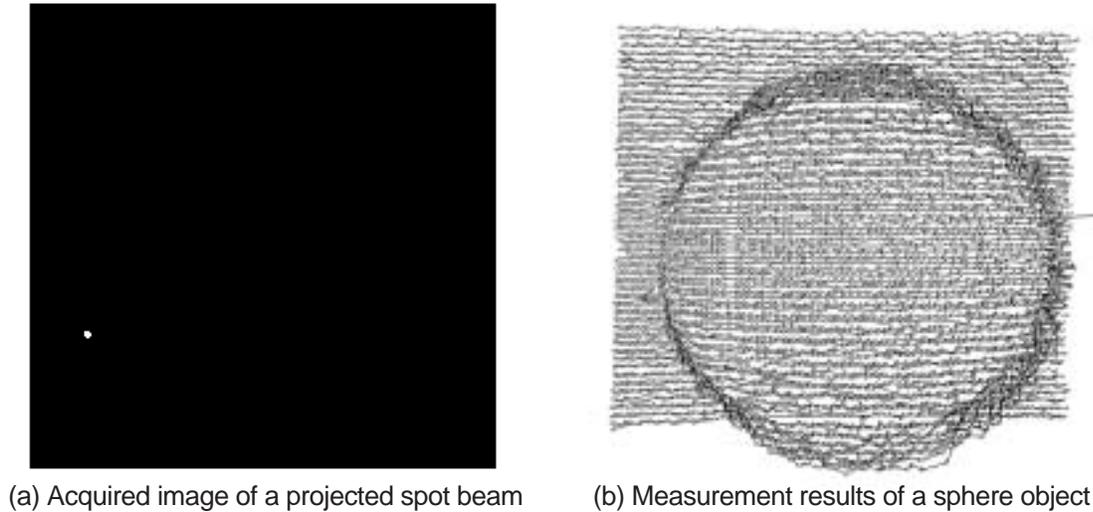


Figure 8. Measurement results of the quad-tree scan sensor.

3.3 Comparison

3.3.1 Position Detection Speed

In this section, we compare the quad-tree scan position sensor with a conventional position sensor [10] and a high-speed 2-D image sensor [13]. Our sensor and [10] are suitable for a spot-beam-projection system since they are customized to detect a few activated pixels in a large pixel array. A spot-beam-projection system requires $N \times N$ frames for a range map. Therefore it is suitable for tracking and position adjustment applications with range data rather than 3-D imaging applications.

The quad-tree scan position sensor achieves 10k points/s in 256×256 pixels, which corresponds to 10k range data/s. As a tracking sensor, it achieves 10k fps without limitation of a target moving speed. On the other hand, the conventional sensor [10] is customized for a tracking application. It has 2-D winner-take-all circuits by analog circuit techniques to detect the position of an incident spot beam. It achieves 7k pixels/s tracking in 24×24 due to search area prediction. However it loses a target out of 3×3 prediction area if a target moves in higher speed. The high-speed 2-D image sensor has a possibility of 500 fps spot-beam tracking.

3.3.2 Range Accuracy

Range accuracy is mainly determined by a measurement setup and a sensor resolution. In terms of a measurement setup, the range accuracy depends on a parallax of triangulation, a distance of target objects from a camera, and accuracy of optical setup such as a lens and a scanning mirror. Therefore a sensor resolution is a unique factor of range accuracy among 3-D image sensors. The sensor resolution is provided by not only the pixel resolution but also the sub-pixel resolution of position detection. The sub-pixel center position can be acquired by gravity center calculation using a couple of activated pixels on the sensor plane.

The pixel size of our quad-tree scan sensor is $28 \times 28 \mu\text{m}^2$ with 22.1 % fill factor in $0.6 \mu\text{m}$ CMOS process. The quad-tree scan architecture is implemented by digital circuit techniques, so it can be applied to a larger pixel array. The quad-tree position sensor utilizes binary data to get the position of a spot beam. Assuming 5 – 10 pixels are activated, the sub-pixel resolution is 0.1 – 0.2 pixels. On the other hand, the pixel size of the conventional sensor [10] is $62 \times 62 \mu\text{m}^2$ with 30.0 % fill factor in $2.0 \mu\text{m}$ CMOS process. The sub-pixel resolution of the sensor [10] for a spot beam is 1.0 pixels since it detects the center position using analog 2-D winner-takes-all (WTA) circuits. The 2-D WTA circuits are unsuitable for scaling of the transistor size in the future. Thus it is difficult to keep the high-speed position detection in larger pixel array. The comparisons are summarized in Table II.

Table II. Performance Comparison.

	frame rate	limitation	sub-pixels	# pixels	pixel pitch	process
Our quad-tree scan sensor	10k fps	none	0.1 - 0.2 pixels	256 × 256	28.0 μm	0.6 μm CMOS
Brajobic (JSSC '98) [10]	7k fps	< 7k pixels/s	1.0 pixels	24 × 24	62.0 μm	2.0 μm CMOS
Krymski (Symp.VLSI '99) [13]	500 fps	none	N/A	1024 × 1024	10.0 μm	0.5 μm CMOS

4 SMART ACCESS IMAGE SENSORS FOR SHEET-BEAM-PROJECTION SYSTEM

4.1 Principle of 3-D Measurement with Sheet Beam Projection

Figure 9 shows an example of range finding system based on the light-section method using sheet beam projection. The range finding system basically consists of a sheet beam source and a sensor for position detection as shown in Figure 9 (a). The range data of a target object are acquired by triangulation using the projected beam direction and the position of incident beam on the sensor plane as well as a system with spot beam projection described in Section 3.1. For example, the positions of reflected beam on the sensor plane are different when a target object is placed in different locations as shown in Figure 9 (b). The scanning direction is X-axis and a sensor detects the center line positions of an incident sheet beam on the sensor plane. A 3-D measurement system with sheet beam projection reduces the number of required frames for a range map since it needs N frames of position detection with $N \times N$ pixel resolution. It enables to realize a high-speed range finding system. On the other hand, much more pixels are activated on the sensor plane than that of a spot-beam-projection system. In Section 4, three position sensors for sheet beam projection are presented to achieve high-speed and high-resolution 3-D measurement.

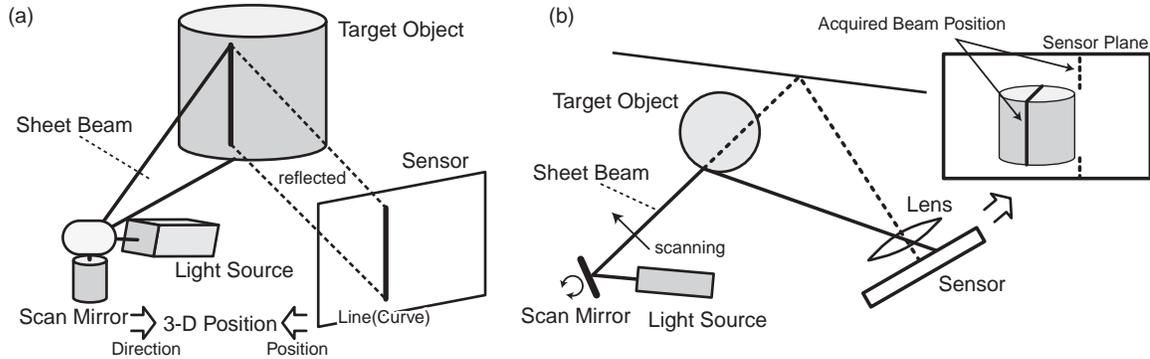


Figure 9. Example of range finding system based on a light-section method: (a) birds-eye view, (b) top view.

4.2 Row-Parallel Position Sensor With Chained Activated Pixel Search Method

In this section, a row-parallel sensor architecture for high-speed position detection of a projected sheet beam is presented. A 3-D measurement system with sheet beam projection reduces the number of frames per range map. On the other hand, it requires a high-speed position detection scheme for an incident sheet beam on the sensor plane since the quad-tree scan method in Section 3.2 is not suitable for position detection of many activated pixels. A sensor recognizes some pixels with strong incident intensity as the history of the scanning sheet beam as shown in Figure 10. Therefore it is important to quickly detect the position of the activated pixels in each row. In our row-parallel search architecture, the position of activated pixels are quickly detected by a row-parallel chained search circuit in pixel and a row-parallel address acquisition of $O(\log N)$ cycles in N -pixel horizontal resolution. The row-parallel position sensor consists of three parts: a row-parallel search part in pixel, a row-parallel address acquisition part, and a row-parallel processor part as shown in Figure 11 (a).

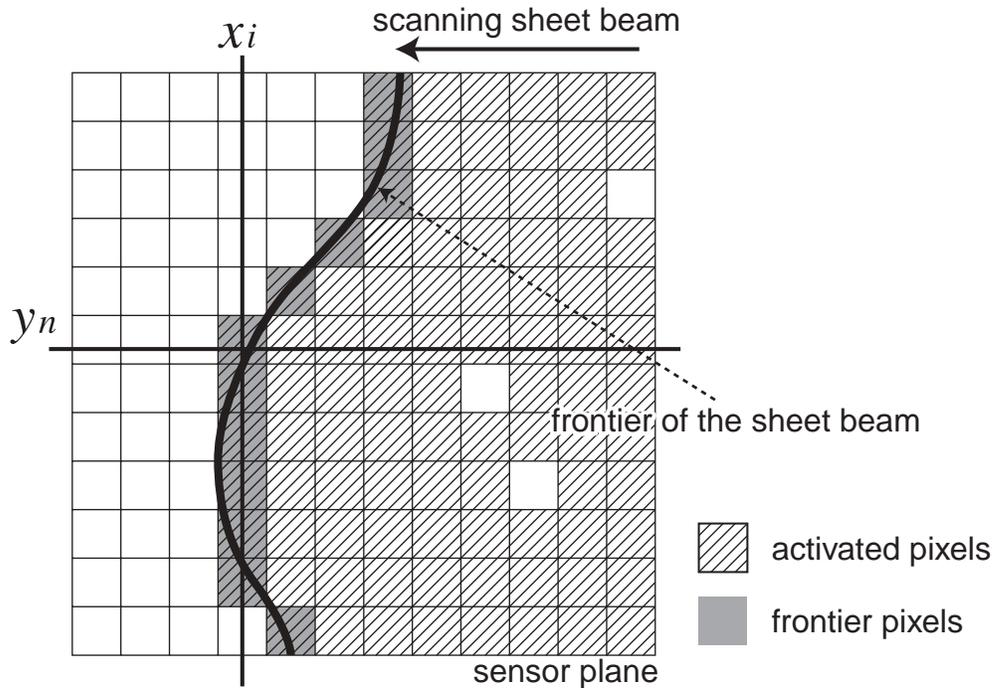


Figure 10. Captured image example of a sheet beam.

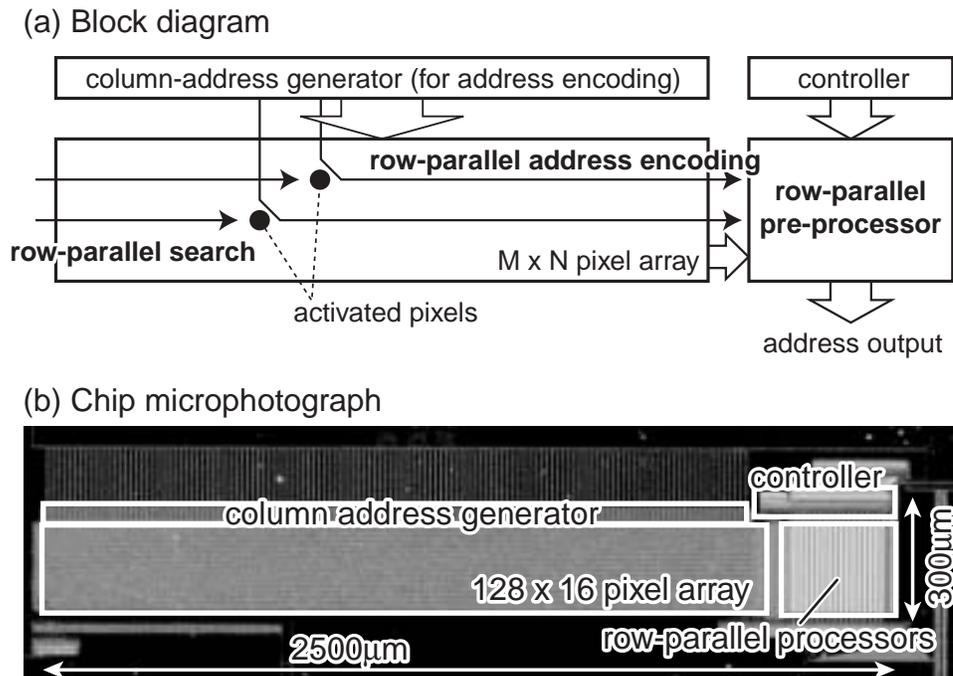


Figure 11. Block diagram and chip microphotograph.

4.2.1 Row-Parallel Architecture and Implementation

We have designed and fabricated a prototype position sensor in 0.35 μm CMOS process. Figure 11 (b) shows a microphotograph of the fabricated chip. It consists of a 128×16 pixel array, a column address generator, row-parallel processors with 32 bit SRAM per row and a memory controller. The pixel circuit

has 1 photo diode and 18 transistors as shown in Figure 12 in $16.25 \mu\text{m} \times 16.25 \mu\text{m}$ pixel area with 20.15 % fill factor. The position sensor occupies $2.5 \text{ mm} \times 0.3 \text{ mm}$ area. The specifications are summarized in Table III.

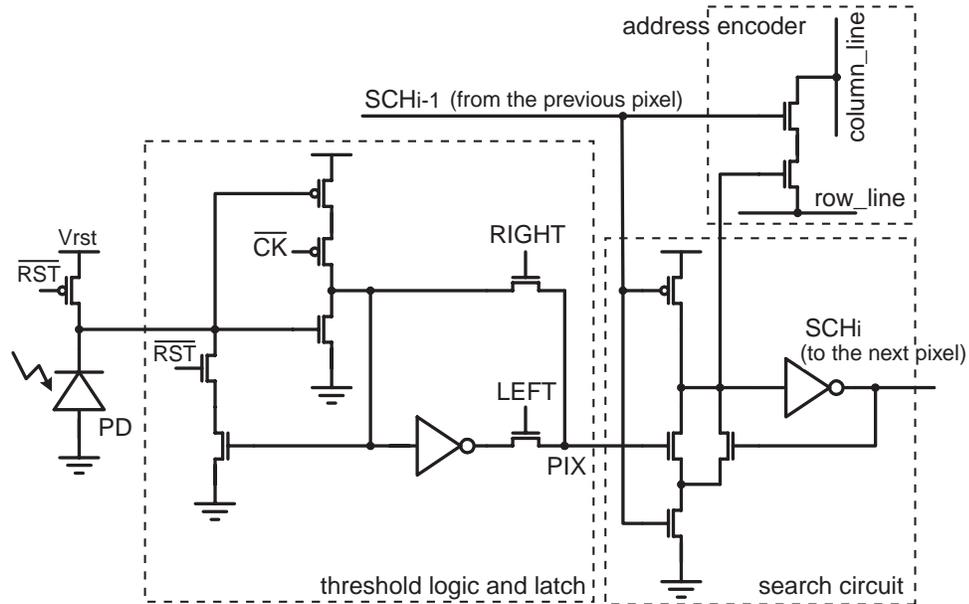


Figure 12. Block diagram of our sensor architecture.

Table III. Specifications of the prototype chip.

Process	0.35 μm CMOS 3-metal 1-poly-Si
Sensor size	2.5 mm \times 0.3 mm
# pixels	128 \times 16 pixels
Pixel size	16.25 μm \times 16.25 μm
# trans. / pixel	18 transistors
Fill factor	20.15 %

The pixel circuit has a photo diode with a reset transistor, a latch circuit with a threshold logic, a search circuit, and an address acquisition circuit as shown in Figure 12. The pixel value at a photo diode is digitized by a threshold logic. V_{rst} is a reset voltage and it enables to change the threshold margin. The pixel activation rate becomes faster when the reset voltage V_{rst} is set to lower. It is limited by S/N caused by fluctuation of the threshold level and a non-uniform ambient incident light. The latch circuit can invert the pixel value PIX using an XOR circuit. At the search circuit, the search signal SCH_{i-1} from the previous pixel passes to the next pixel when PIX is '1'. On the other hand, it stops when PIX is '0'. That is, it stops at the first-detected pixel with strong incident intensity as shown in Figure 11 (a). The address of the detected pixel is acquired in row parallel using two pass transistors. The next search period using inverted pixel values provides the activated right edge to get the center position of the projected beam. In addition, the positions of the second and more activated pixels are detectable by the iteration of PIX inversions.

The address acquisition circuit of the pixel circuit consists of only 2 pass transistors as shown in Figure 12. At the detected pixel of each row, the column line is connected to the row line via the pass transistors as shown in Figure 13. Then, the serial-bit-streamed column address is injected to each column line in parallel. The address of the detected pixel runs into each row line through the pass transistors. In each row, a row-parallel preprocessor receives the serial-bit-streamed address. Therefore the address acquisition cycles are $O(\log N)$ in N -pixel horizontal resolution. The compact pixel circuit implementation and the high-speed row-parallel address acquisition contribute quick position detection in high pixel resolution.

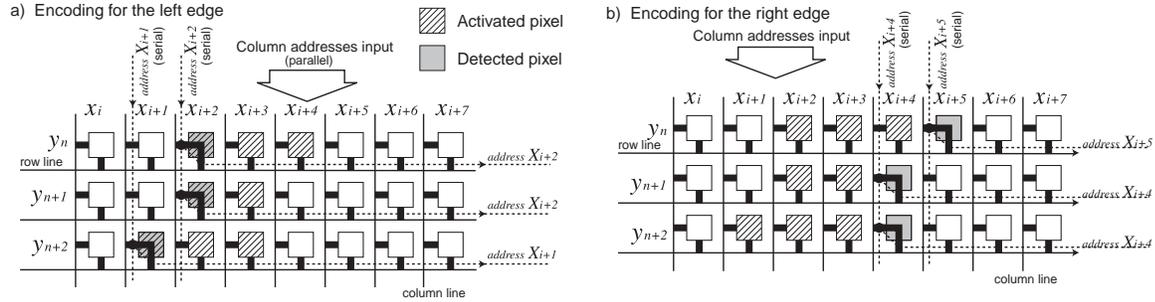


Figure 13. Method of row-parallel address acquisition.

The address outputs are received by row-parallel processors as shown in Figure 11 (a). The row-parallel processor consists of a full adder, random access memories with a read/write circuit, output buffers for pipe-lined data readout, and some control logics. The addresses of x_i and x_{j+1} are acquired in the row-parallel address acquisition when the edges of the activated pixels are x_i and x_j .

The processor calculates the center position of the detected pixels and reduces data transmission. And also it realizes to get the positions of multiple sheet beams in one frame.

4.2.2 Measurement Results

The measurement system consists of the fabricated position detector on a test board, a scanning mirror with 300 mW laser beam source (665 nm wavelength), an FPGA for system control, and a host PC. The FPGA was operated at 80 MHz due to the limitation of the testing equipment. In this case, the search time was 450 ns per frame and the photo integration time was 30 μ s at $V_{rst} = 1.4$ V. Figure 14 (a) shows sequentially captured positions of the scanning sheet beam of 2 kHz by a reset-per-frame mode. In a reset-per-frame mode, the operation of position detection is carried out after the integration with reset operation. Here the position detector provides the center address calculated by the row-parallel processor. The measurement result shows that the access rate f_{acc} of activated pixels is 2.22 MHz and the pixel-activation rate f_{pa} is 33.3 kHz. The frame interval takes 30.9 μ s per frame ($f_{ps} = 32.2$ k fps), which includes 30.0 μ s integration time. 256 sub-pixel resolution is realized by the center calculation to improve the range accuracy. Figure 14 (b) shows the frontier positions of the scanning sheet beam during photo current integration in a reset-per-scan mode. In a reset-per-scan mode, the activated frontier positions of the scanning beam are detected during the integration. In the measurement situation, 2 kHz mirror scanning within the camera angle is limited by a scan drive of galvanometer mirror. The pixel-activation rate of a reset-per-scan mode is around 233 kHz in our measurement system. That is, the possible frame rate f_{psd} of the system with 128-pixel horizontal resolution is 233k fps limited by the intensity of projected beam.

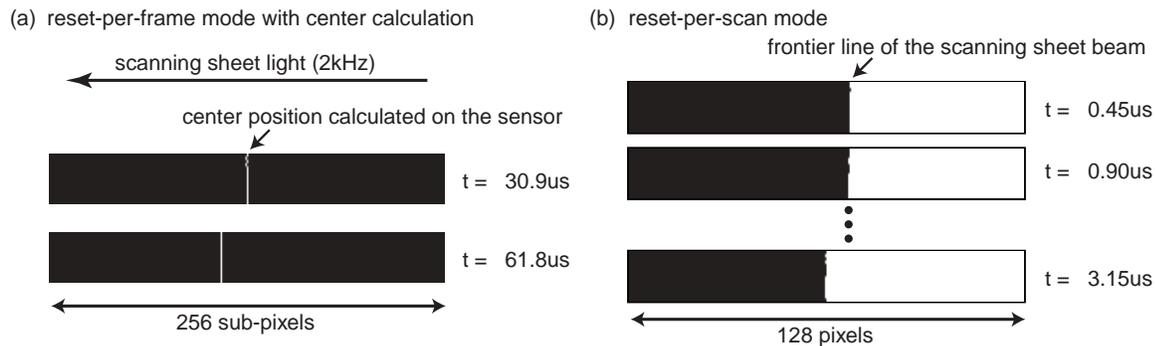


Figure 14. Measurement results.

4.2.3 Summary

A row-parallel sensor architecture and its circuit implementation have been proposed for a high-speed 3-D camera using the light-section method. In the measurement results of the 128 \times 16 prototype position

sensor, the access rate of activated pixels achieves 2.22 MHz. We have shown 32.2k-fps and 233k-fps position detection with 2 kHz scanning beam of 300 mW in a reset-per-frame mode and a reset-per-scan mode respectively. The possible frame rate is 2.22M fps with sufficient beam intensity. It has the capability of quick position detection to realize a high-speed 3-D camera for “beyond-real-time” range finding and visual feedback such as 1000 range maps/s. Now we have successfully developed a 375×365 3-D image sensor with the capability of 1052 fps range finding using the present row-parallel architecture [20].

4.3 Row-Parallel Position Sensor With Binary Tree Scan and Mask Method

In this section, we propose a novel image scan method using row-parallel binary-trees as data paths to image data. Figure 1 (c) shows the concept of row-parallel binary-tree scan. In row-parallel binary-tree scan, the positions of activated pixels are detected in parallel in each row. Assuming that only one pixel is activated in each row of an $N \times N$ pixel sensor, the number of scan cycles of the row-parallel binary-tree scan increases with order of $N \times \log N$. Compared with a raster scan method with $O(N^2)$ cycles, it achieves few cycles for high-resolution range finding. For example, the required cycle time of image scan in the raster scan and the binary-tree scan are 16 ps and 1.5 μ s respectively in 60 range maps/s of 1024×1024 pixels. The feature of row-parallel binary-tree scan realizes 3-D measurement with both high speed and high resolution.

4.3.1 Row-Parallel Binary-Tree Scan

The row-parallel binary-tree scan can be implemented on the sensor plane by scan controllers with a binary-tree structure in each row. However, the amount of hardware becomes too large using such direct implementation. So, we considered about a procedure of row-parallel binary-tree scan for efficient implementation on the sensor plane. Figure 15 shows the procedure of row-parallel binary-tree scan. Each pixel has a mask register to mask the pixel output. The positions of activated pixels in each row are detected from left to right. Here, we explain the procedure using an example in Figure 15. (a) Scan starts with resetting all mask registers. (b) Select all pixels and acquire OR of pixel values in each row to detect completion of scan. (c) Select the left half plane of the pixel array and acquire OR of pixel values. Here, the output of each row indicates the inversion of the position’s MSB of the leftmost activated pixel. (d) Mask right half plane of pixel array with “1” output in step (c). (e) Select even columns of the pixel array and acquire OR of pixel values. Here output of each row indicates inversion of position’s LSB of the leftmost activated pixel. (f) Mask the odd columns of the pixel array with “1” output in step (e). (g) Reset pixels without mask to avoid rescanning scanned pixels. (h–n) Repeat the same procedure and detect the positions of the second leftmost pixels. (o–p) Finish the scan procedure when all activated pixels are scanned. We can efficiently realize the procedure using one address decoder outside pixel array and one mask register in each pixel.

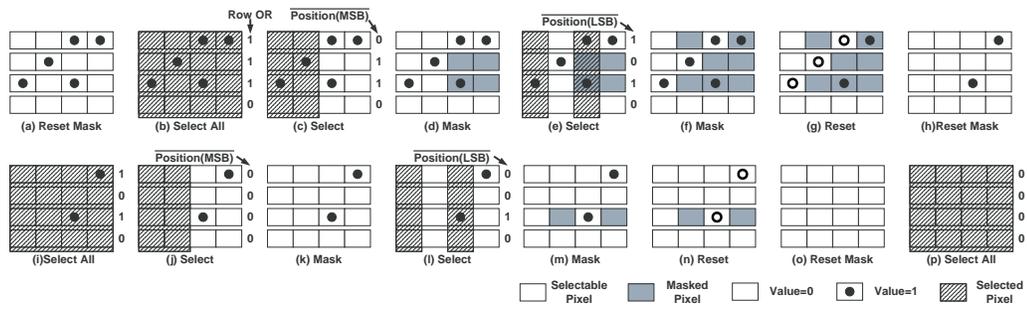


Figure 15. Procedure of row-parallel binary-tree scan.

4.3.2 Circuit Implementation

We have designed a smart position sensor with the row-parallel binary-tree scan method. Figure 16 shows the microphotograph of the fabricated sensor. Table IV shows the summary of the sensor. The sensor has been fabricated using 0.35 μ m CMOS 3-metal 2-poly-Si process. The sensor has a 128×128 pixel array, an address decoder, row-parallel mask controllers, row-parallel serial/parallel converters and a position register.

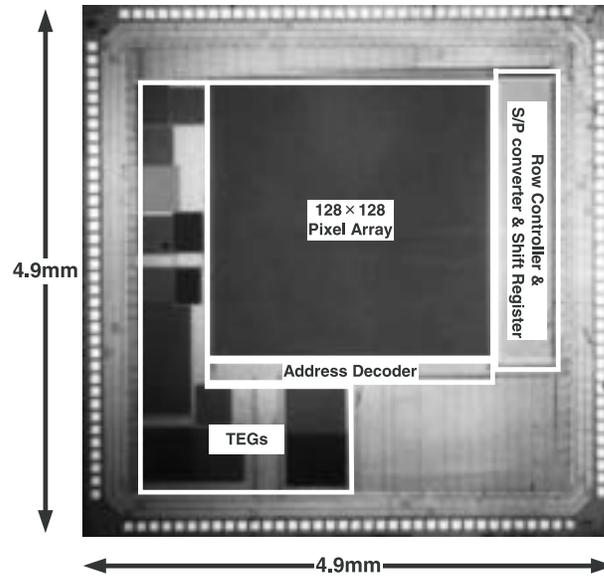


Figure 16. Chip microphotograph.

Table IV. Specifications of the fabricated sensor.

Process	0.35 μm CMOS 3-metal 1-poly-Si
Die size	4.9 mm \times 4.9 mm
# pixels	128 \times 128 pixels
Pixel size	19.5 μm \times 19.5 μm
# trans. / pixel	28 transistors
Fill factor	7.1 %
Power dissipation	344 mW (@ Vdd=3.3V, 44.4M cycles/s)

Figure 17 shows a pixel circuit and a row-parallel scan controller. A pixel is composed a photo detector, a 1-bit latch, a mask register and an output circuit. The reset transistor resets the output of the photo detector to V_{ref} . After integration of photo current, the latch converts the output of the photo detector to a 1-bit binary value. When the mask register is set, the register masks the output of the pixel. The output circuit is a part of a wired-OR circuit. The output circuits of pixels in a row and the precharge transistor compose a wired-OR circuit. The precharge transistor precharges the output of the wired-OR to the precharge voltage V_{pre} , which is 200mV above the threshold voltage of the latch. The 1-bit latch senses the output of the wired-OR. The mask control logic controls all pixels in one row and is simply composed of a NAND gate. A ripple OR circuit detects completion of scan.

4.3.3 Measurement Results

The measurement system of the row-parallel binary-tree scan sensor is based on the light-section method with sheet beam projection. Figure 18 (a) shows a gray scale image acquired by the sensor. Here, we scanned 255 times using raster scan during photo current integration and converted data to an 8-bit gray-scale image data. Figure 18 (b) shows a range image measured in the row-parallel binary-tree scan. We measured a model train under a normal room light. Figure 18 (c) shows a 3-D image with texture in Figure 18 (a). Figure 18 (d) shows the 3-D measurement result of a moving object. We measured a moving hand at the speed of 12 range maps/s. We note that the measurement speed is limited by digital I/O boards on a host PC in the measurement setup. The integration time is 200 μs . Therefore we can achieve 40 range maps/s using a faster controller. And more efficient photo detectors such as pin photo diodes can provide the capability of higher-speed 3-D measurement. By the result of circuit simulation, the maximum 3-D

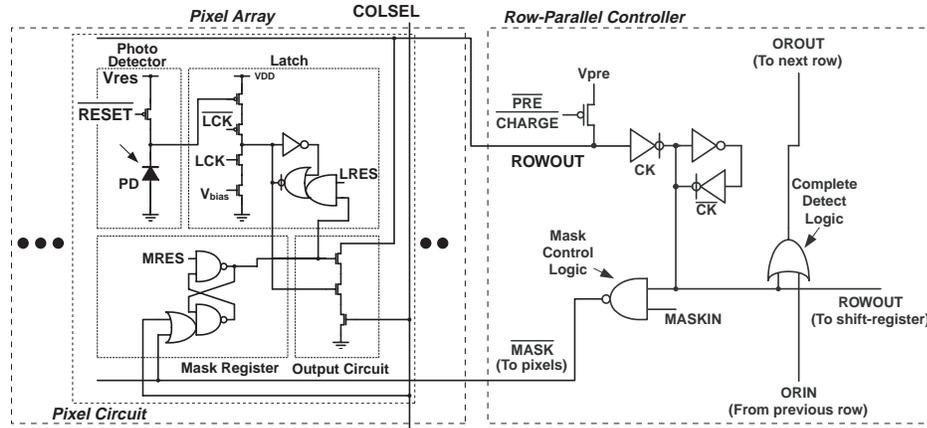


Figure 17. Schematic of a pixel circuit and a row-parallel scan controller.

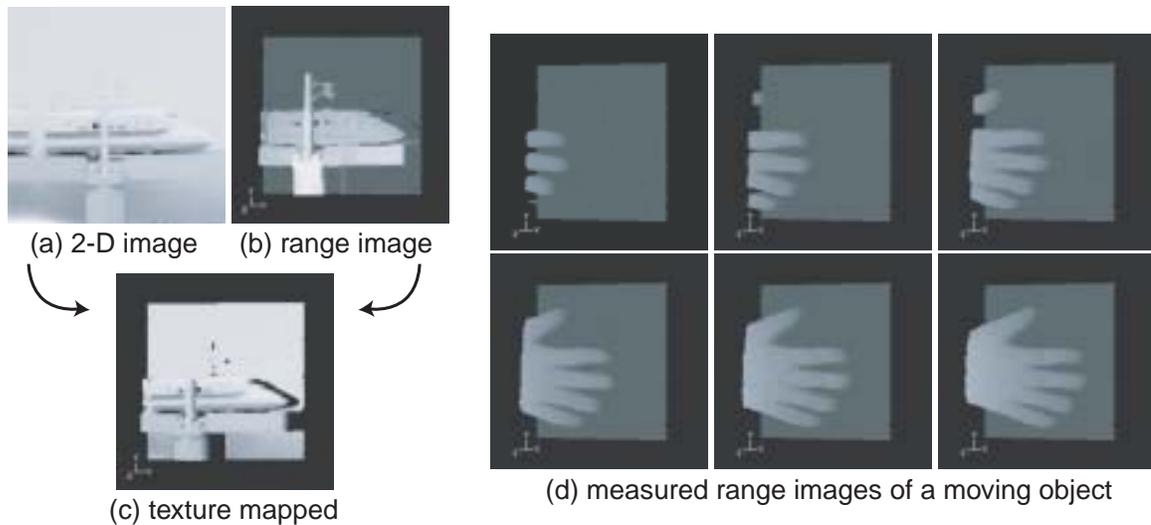


Figure 18. Measurement results.

measurement speed is 24.3k range maps/s. Assuming a 1024×1024 pixel sensor, we can achieve 593 range maps/s. In an ideal measurement setup, the range accuracy in 1 sampling and 16 samplings is 1.8 mm and 0.4 mm respectively at a distance of 1000 mm with 200 mm base line between the camera and the beam projector.

4.3.4 Summary

We proposed a row-parallel binary-tree scan method and its efficient implementation method. Positions of a projected sheet beam are detected with a small number of scan cycles in comparison with conventional scan methods. We have developed a smart position sensor with the row-parallel binary-tree scan. We measured moving objects at the speed of 12 range maps/s using the fabricated sensor. The possible range accuracy is 0.4 mm at a distance of 1000 mm by center position calculation with 16 samplings. By the result of circuit simulation, it can achieve 593 range maps/s with 1024×1024 pixels.

4.4 Column-Parallel Position Sensor With High-Speed Line-at-a-Time Readout

The smart access methods described in Section 3.2 – Section 4.3 are efficient for high-speed position detection and range finding. Especially our row-parallel access methods have the capability of around 1000 range maps/s with high pixel resolution for a future high-speed camera. On the other hand, they have scan circuits in pixel, so the pixel resolution is limited by their pixel size. To realize “real-time” 3-D

applications with high pixel resolution, which require 30 – 60 range maps/s, it is important to decrease a pixel circuit. In this section, we propose two techniques for a column-parallel scan method with line-at-a-time readout to realize high-resolution and real-time range finding: a high-speed readout scheme and a column-parallel position detector. The high-speed readout scheme using adaptive thresholding and time-domain approximate ADCs achieves high frame rate for real-time range finding and high range accuracy due to sub-pixel position calculation. In addition, it allows a standard and compact pixel circuit for high pixel resolution. The column-parallel position detector suppresses redundant data transmission for a real-time measurement system. We have developed the first real-time range finder with the capability of VGA (640×480) resolution based on the light-section method.

4.4.1 Sensor Architecture and Circuit Implementation

Figure 19 shows the circuit configuration and the sensing scheme of our column-parallel scan method with adaptive thresholding. It consists of an adaptive thresholding circuit and time-domain approximate ADCs (TDA-ADC) in column parallel. In 3-D imaging mode, a row line is accessed using a dynamic readout scheme after precharged as shown in Figure 19(c)–(1). Some pixels, where a strong light incidents, are detected when the pixel value is over the threshold level decided by dark pixel values adaptively. Here the pixel values are estimated in time domain as shown in Figure 19(c)–(3). In the same operation, the intensity profile of activated pixels is acquired by the time-domain ADCs to improve sub-pixel accuracy as shown in Figure 19(c)–(2). The adaptive thresholding circuit suppresses overall ambient light intensity and fluctuation of access speed in each row. Moreover the threshold level and the resolution of ADCs are controllable by some external voltages, V_{rst} , V_{pc} and V_{cmp} after fabrication.

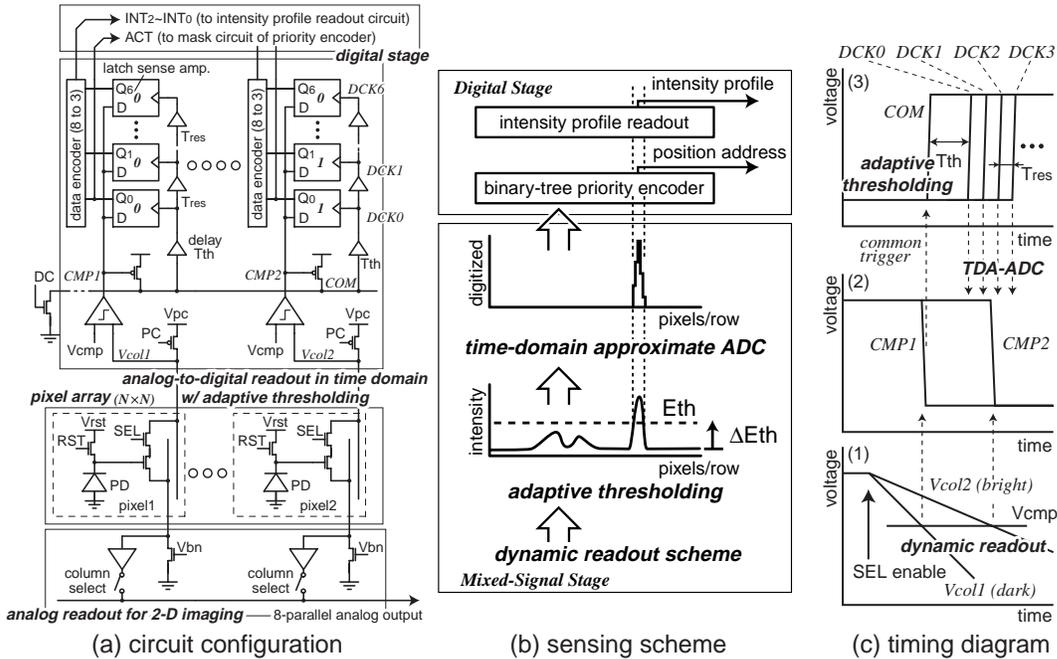


Figure 19. Circuit configuration and sensing scheme.

A binary-tree priority encoder (PE) receives ACT from the adaptive thresholding circuit. It consists of a mask circuit, a binary-tree priority decision circuit and an address encoder. At the mask circuit, ACT_n is compared with the neighbors ACT_{n+1} and ACT_{n-1} to detect the left and right edges using XOR circuits. The priority decision circuit receives the inputs from the mask circuits and generates the output at the minimum address of activated pixels. The addresses of the left and right edges are encoded at the address encoder. After the first-priority edge has been detected, the edge is masked by the output of the priority decision circuit. And then the location of the next priority of activated pixels is encoded. Our improved priority decision circuit keeps high speed in large input number due to a binary-tree structure and a compact circuit cell. Its delay increases in proportion to $\log N$, where N is input number.

4.4.2 Chip Implementation

We have designed and fabricated a 640×480 range finder using the present architecture and circuit in $0.6 \mu\text{m}$ CMOS process. Figure 20 shows the chip microphotograph and components. The sensor has a 640×480 pixel array, row select and reset decoders, 2-D image readout circuit, column-parallel TDA-ADCs, a 640-input priority encoder and an intensity profile readout circuit in $8.9 \text{ mm} \times 8.9 \text{ mm}$ die size. The pixel has a photo diode and 3 transistors. The area is $12.0 \mu\text{m} \times 12.0 \mu\text{m}$ with 29.5% fill factor. Table V shows the specifications of the fabricated sensor.

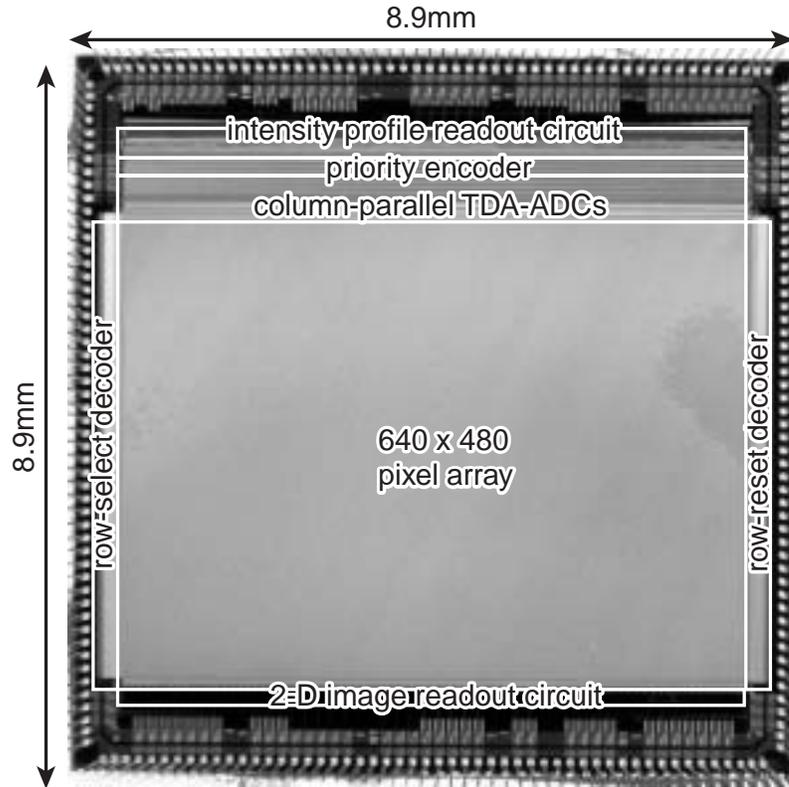


Figure 20. Chip microphotograph.

Table V. Specifications of the fabricated sensor.

Process	$0.6 \mu\text{m}$ CMOS 3-metal 2-poly-Si
Die size	$8.9 \text{ mm} \times 8.9 \text{ mm}$
# of pixels	640×480 pixels (VGA)
# of transistors	1.12M transistors
Pixel size	$12.0 \mu\text{m} \times 12.0 \mu\text{m}$
# of trans. / pixel	3 transistors
Fill factor	29.54 %

4.4.3 Measurement Results

In 2-D imaging, 8 pixel values are readout in parallel and it takes $2 \mu\text{s}$. The maximum 2-D imaging speed is 13 fps (frames/s) using 8-parallel high-speed external ADCs. It has a potential of higher speed of 2-D imaging since it is easy to implement the conventional readout techniques for 2-D imaging in our sensor architecture.

In 3-D imaging, the measurement system is composed of the camera with the fabricated sensor, a laser (wavelength 665 nm) with a rod lens for beam extension, a scanning mirror with a DAC, an ADC for 2-D imaging, an FPGA for sensor control, and a PC for display. Activated pixels in a row line are accessed and

detected within 50 ns. The delay time of the priority encoder stage is 17.2 ns for the left and right edges. The readout time of the intensity profile is 21.5 ns. Their stages are pipelined. Therefore the location of the projected sheet beam is acquired in 24.0 μ s. The range finder realizes 65.1 range maps/s in VGA pixel resolution.

The standard deviation of measured error is 0.26 mm and the maximum error is 0.87 mm at a distance of 1170 mm – 1230 mm by gravity center calculation using an acquired intensity profile when we measured the distance of a white flat board. For comparison, the standard deviation of measured error is 0.54 mm and the maximum error is 2.13 mm by the conventional binary-based position calculation. Table VI shows the performance of the sensor.

Table VI. Performance of the present sensor.

Power supply voltage	5.0 V
Power dissipation	305 mW (@ 10 MHz)
Max. 2-D imaging rate	13.0 frames/sec
Max. position detection rate	41.7k lines/sec
Max. range finding rate	65.1 range maps/sec
Range accuracy (max. error)	0.87 mm @ 1200 mm

Figure 21 shows measured images by the present range finder. Figure 21 (a) is a captured 2-D image of a hand. Figure 21 (b)–(d) are its range maps. The brightness of the range maps represents the distance from the range finder to the target object. The range data has been already plotted in 3-D space, so it can be rotated freely as shown in Figure 21 (b)–(d). Figure 21(e) is a wire frame reproduced by the measured range data and Figure 21(f) is a close-up of Figure 21(e). The measured images show that our range finder with VGA pixel resolution realizes high-resolution 3-D imaging.

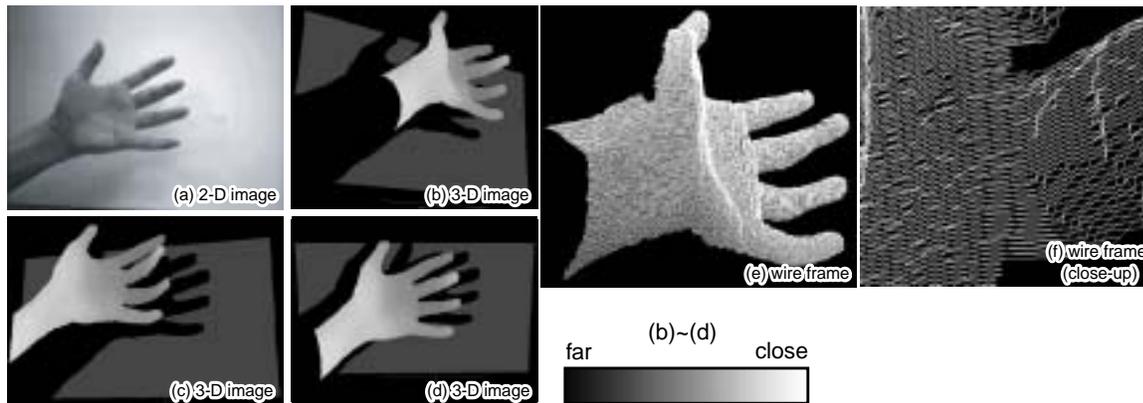


Figure 21. Measurement results of the present sensor.

4.4.4 Summary

A 640×480 real-time 3-D image sensor using a high-speed readout scheme and a column-parallel position detector has been presented. It is the first 3-D image sensor based on the light-section method to realize VGA pixel resolution and real-time range finding. Our high-speed readout scheme realizes to use a standard and compact pixel circuit and to get the location and intensity profile of a projected sheet beam on the sensor plane quickly. The column-parallel position detector suppresses redundant data transmission for a real-time measurement system. The maximum range finding speed is 65.1 range maps/sec. The maximum range error is 0.87 mm and the standard deviation of error is 0.26 mm at 1200 mm distance due to an intensity profile. A 2-D image and a high-resolution 3-D image have been acquired by the 3-D measurement system using the present image sensor.

4.5 Comparison Among Smart Access Methods

4.5.1 Range Finding Speed

In this section, we consider a possible range finding speed of the reported image sensors. Frame rate depends on cycle time and the number of cycles for range finding. Cycle time increases in proportion to pixel resolution due to the pixel access load in general though the trend of cycle time itself is different in each readout scheme. It is common aspect among our smart access sensors and the conventional sensors. On the other hand, the trend of required cycles for a range map is particularly different in each readout scheme.

Figure 22 shows the dependence of the number of scan cycles on the number of pixels, assuming only one pixel is activated in each row and the range finding speed is 60 range maps/s with the same number of range data as pixels. The number of scan cycles in raster scan, which is a scan method of a standard CCD and a CMOS APS, increases with order of N^3 as shown in Figure 22. On the other hand, it increases with order of N^2 in column-parallel scan with line-at-a-time readout, which is implemented on our 3-D image sensor in Section 4.4 and some 3-D image sensors [16, 17]. To realize real-time range finding with high pixel resolution using a column-parallel scan method, the high-speed cycle time of line-at-a-time readout is required in high pixel resolution. Therefore the sensors [16] has a pixel-parallel ADC for high-speed binary image readout, and our image sensor in Section 4.4 has a high-speed readout scheme with adaptive thresholding. In row-parallel scan of Figure 22, the number of scan cycles increases with order of $N \times \log N$, which is estimated by our row-parallel binary-tree sensor in Section 4.3. The row-parallel scan architecture in Section 4.2 and the conventional one [15] also follow the similar dependence basically.

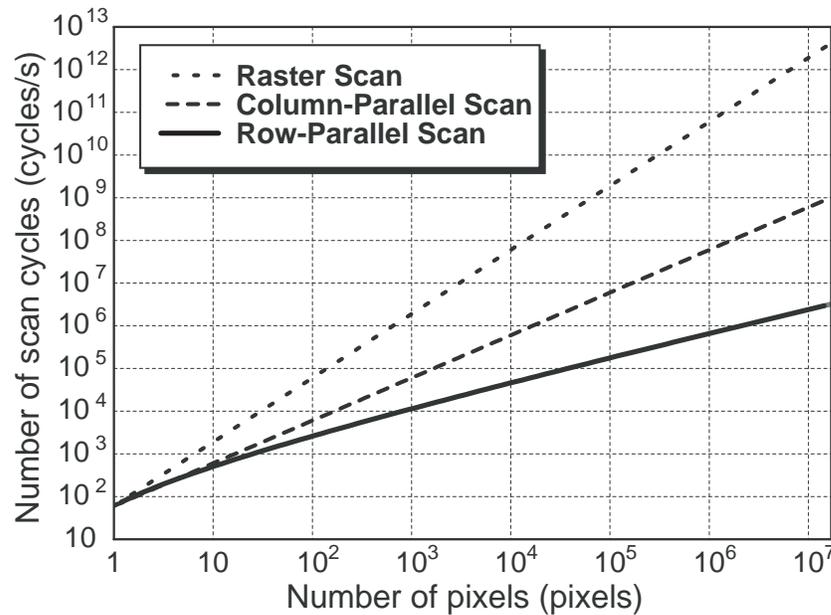


Figure 22. Dependence of the number of scan cycles on the number of pixels (sheet beam projection @ 60 fps).

Figure 23 shows comparison among our image sensors and the conventional sensors [13], [15]–[17]. [13] is a reference as a high-speed column-parallel 2-D image sensor with 1M pixel resolution, not customized for 3-D imaging. Black plots in Figure 23 represent the reported range finding speeds. White plots represent the possible range finding speeds, assuming a measurement system has a plenty strong beam and a high-speed sensor controller. The smart access sensors with row-parallel scan in Section 4.2 and Section 4.3 have the capability of ultra high-speed 3-D imaging up to 1000 range maps/s though their pixel resolutions are currently low. On the other hand, our 3-D image sensor with column-parallel scan in Section 4.4 achieves 640×480 pixel range finding in 60 range maps/s due to compact pixel circuit implementation with 1 PD and 3 FETs.

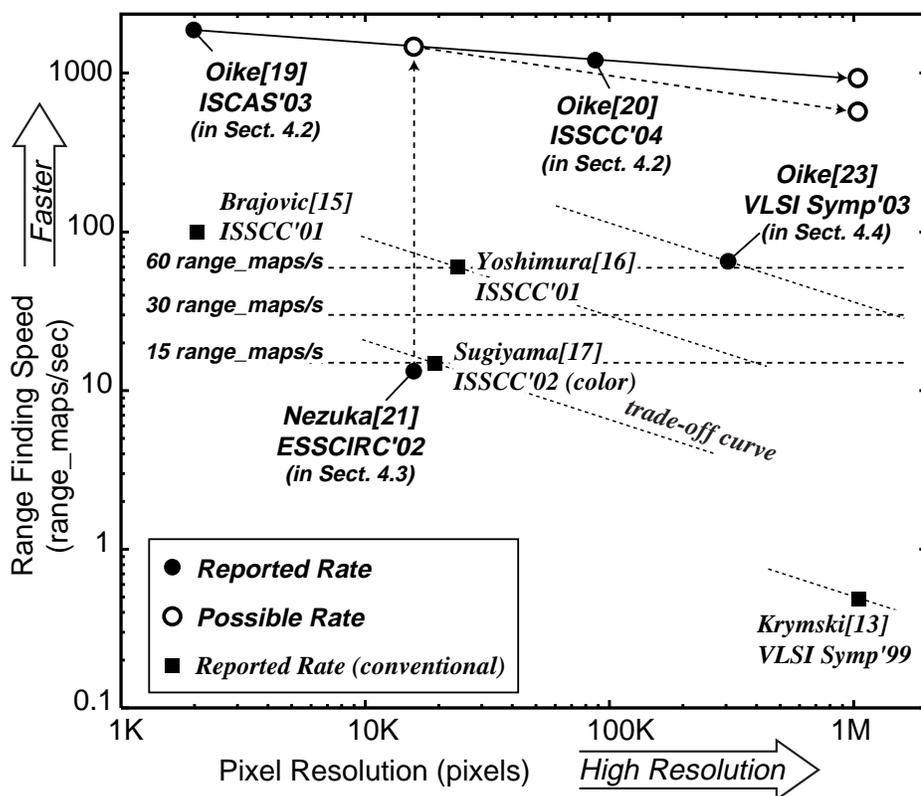


Figure 23. Range finding speed and pixel resolution.

4.5.2 Pixel Resolution

Pixel resolution is limited by a die size, a pixel size and a scan architecture. It is difficult for some position sensors based on analog processing [10]–[15] to follow the pixel resolution increase since the SNR of analog processing for position detection decreases in proportion to pixel resolution. Our image sensors and the other conventional sensors [16]–[17] can achieve higher pixel resolution as the process technology proceeds. Table VII shows the comparison of the number of transistors per pixel. A pixel size depends on the number of transistors, the fill factor and the process technology. Basically some sensors, for example our column-parallel sensor and the sensor [17], keep advantage of high pixel resolution due to compact pixel circuit implementation though the process technology proceeds. On the other hand, [24] reported the scaling limitation of pixel size due to several optical factors in the process technology scaling as shown in Figure 24. Therefore the sensors with large pixel circuits also have the possibility of high pixel resolution equivalent to those with small pixel circuits in the future.

Table VII. Comparison of # FETs / pixel.

	# FETs/pixel	pixel size	fill factor	process
The row-parallel sensor 1 (Sect.4.2)	18 FETs	16.25 × 16.25 μm ²	20.15 %	0.35 μm CMOS
The row-parallel sensor 2 (Sect.4.3)	28 FETs	19.5 × 19.5 μm ²	7.10 %	0.35 μm CMOS
The column-parallel sensor (Sect.4.4)	3 FETs	12.0 × 12.0 μm ²	29.54 %	0.6 μm CMOS
Krymski (Symp.VLSI '99) [13]	3 FETs	10.0 × 10.0 μm ²	45 %	0.5 μm CMOS
Brajovic (ISSCC '01) [15]	> 9 FETs	30.0 × 30.0 μm ²	N/A	N/A
Sugiyama (ISSCC '01) [16]	32 FETs + 2 Cap.	46.4 × 54.0 μm ²	25 %	0.35 μm CMOS
Yoshimura (ISSCC '02) [17]	5 FETs	11.2 × 11.2 μm ²	53 %	0.35 μm CMOS

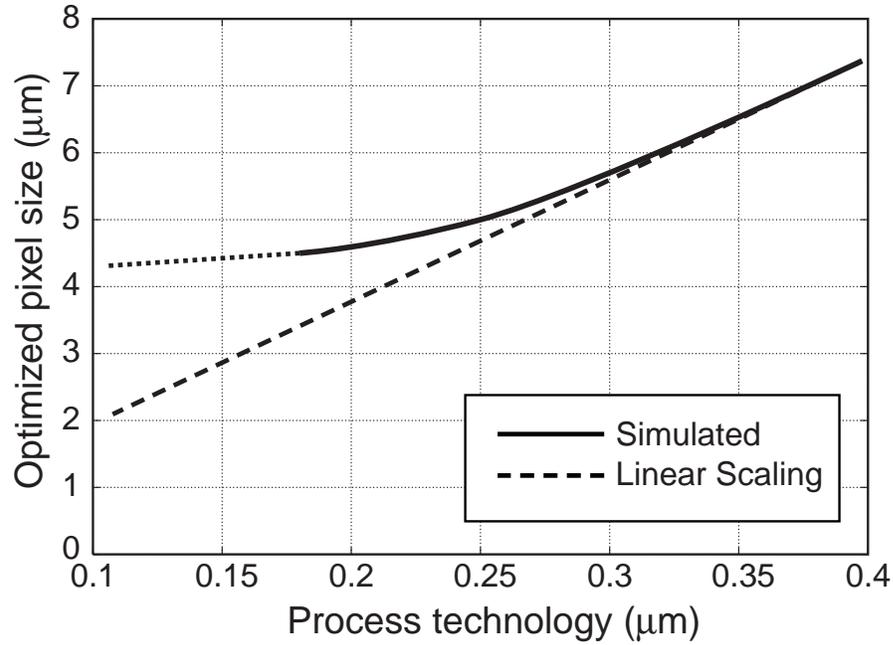


Figure 24. Scaling limitation of pixel size [24].

4.5.3 Range Accuracy

As mentioned in Section 3.3.2, the range accuracy of position sensors are mainly determined by the pixel resolution and sub-pixel resolution. In a sheet-beam-projection system, the sub-pixel resolution is generally 0.5 pixels due to gravity center calculation using a binary image in row. That is, the sub-pixel resolution of a sheet-beam-projection system is less than that of a spot-beam-projection system since the shape of activated pixels by the incident spot beam represents its intensity profile. Therefore position sensors for a sheet-beam-projection system have to acquire the intensity profile of the incident sheet beam to achieve higher sub-pixel resolution.

The sensor [15] achieves 64×64 sensor resolution by 64×32 pixels because of negative/positive peak detections of row-parallel analog WTA circuits. That is, the sub-pixel resolution is 0.5 pixels. Our row-parallel sensors also improve the sensor resolution by multiple samplings and scans per reset as mentioned in Section 4.3.3. Therefore their sub-pixel resolutions depend on the required range finding speed as the same as the sensors [16, 17]. The sub-pixel resolution of the row-parallel sensor in Section 4.3 achieves about 0.12 pixels in 16 samplings. [16] and [17] limit the sub-pixel resolution by the scan rate on the sensor plane since they detect the position of incident beam as the timing of pixel activation. The sub-pixel resolution of [17] corresponds to 0.72 pixels at 15 range maps/s in their measurement setup. Our column-parallel sensor in Section 4.4 has the capability of intensity profile acquisition by time-domain approximate ADCs and its sub-pixel resolution achieves about 0.2 pixels. The possible sub-pixel resolutions are summarized in Figure 25.

5 CONCLUSIONS

We have introduced concepts of smart access methods for quick position detection to realize a high-speed 3-D measurement system with high range resolution based on the light-section method. Our quad-tree scan position sensor achieves 10k points/s range measurement with 0.4 % range accuracy using a spot beam scanner. It is suitable for tracking and position adjustment applications. The row-parallel scan architectures with novel circuit implementation have the capability of ultra high-speed range finding and visual feedback such as 1000 range maps/s. To realize higher-resolution range finding in real time, we have presented a column-parallel position sensor with high-speed line-at-a-time readout scheme. It is the first

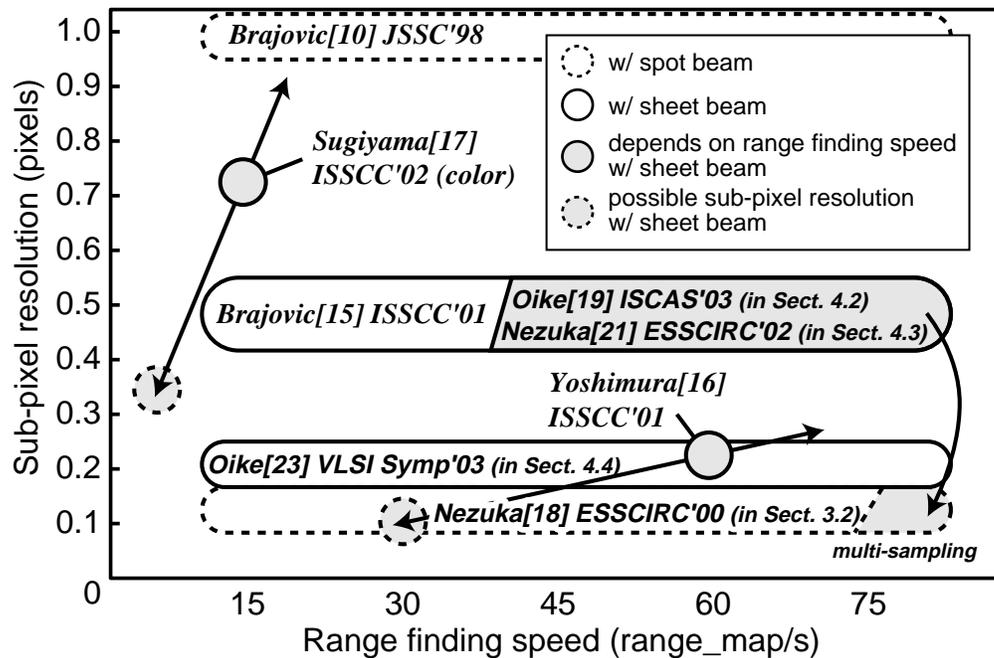


Figure 25. Comparison of possible sub-pixel resolution.

real-time 3-D image sensor with 640×480 pixel resolution and achieves $< 0.1\%$ range accuracy. We have discussed the features and advantages for advanced 3-D imaging applications on the basis of comparison among the smart access methods and the conventional works.

ACKNOWLEDGEMENTS

The VLSI chips in this study have been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), University of Tokyo in collaboration with Rohm Co. and Toppan Printing Co.

REFERENCES

- [1] R. Miyagawa and T. Kanade. 1997. "CCD-Based Range-Finding Sensor," *IEEE Trans. on Electron Devices*, vol. 44, no. 10, pp. 1648 – 1652.
- [2] P. Gulden, M. Vossiek, P. Heide and R. Schwarte. 2002. "Novel Opportunities for Optical Level Gauging and 3-D-Imaging With the Photoelectronic Mixing Device," *IEEE Trans. on Instrumentation and Measurement*, vol. 51, no. 4, pp. 679 – 684.
- [3] R. Jeremias, W. Brockherde, G. Doemens, B. Hosticka, L. Listl, and P. Mengel. 2001. "A CMOS Photosensor Array for 3D Imaging Using Pulsed Laser," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 252 – 253.
- [4] R. Lange and P. Seitz. 2001. "Solid-State Time-of-Flight Range Camera," *IEEE Journal of Quantum Electronics*, vol. 37, no. 3, pp. 390 – 397.
- [5] G. J. Iddan and G. Yahav. 2001. "3D Imaging in the Studio and Elsewhere," in *Proc. of SPIE*, vol. 4298, pp. 48 – 55.
- [6] A. Ullrich, N. Studnicka, and J. Riegl. 2002. "Long-Range High-Performance Time-of-Flight-Based 3D Imaging Sensors" in *Proc. of IEEE Int. Symp. 3D Data Processing Visualization and Transmission*, pp. 852 – 856.
- [7] M. Kawakita, T. Kurita, H. Hiroshi, and S. Inoue. 2002. "HDTV Axi-vision Camera," in *Proc. of Int. Broadcasting Convention (IBC)* pp. 397 – 404.
- [8] L. Viarani, D. Stoppa, L. Gonzo, M. Gottardi, and A. Simoni. 2004. "A CMOS Smart Pixel for Active 3-D Vision Applications," *IEEE Sensors Journal*, vol. 4, no. 1, pp. 145 – 152.

- [9] K. Sato, A. Yokoyama, and S. Inokuchi. 1994. "Silicon Range Finder," in *Proc. of IEEE Custom Integrated Circuits Conference (CICC)*, pp. 339 – 342.
- [10] V. Brajovic and T. Kanade. 1998. "Computational Sensor for Visual Tracking with Attention," *IEEE Journal of Solid-State Circuit*, vol. 33, no. 8, pp. 1199 – 1207.
- [11] M. de Bakker, P. W. Verbeek, E. Nieuwkoop and G. K. Steenvoorden. 1998. "A Smart Range Image Sensor," in *Proc. of European Solid-State Circuits Conference (ESSCIRC)*, pp. 208 – 211.
- [12] Y. Oike, M. Ikeda, and K. Asada. 2004. "A 120 x 110 Position Sensor With the Capability of Sensitive and Selective Light Detection in Wide Dynamic Range for Robust Range Finding," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 246 – 251.
- [13] A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E. R. Fossum. 1999. "A High Speed, 500 Frames/s, 1024 x 1024 CMOS Active Pixel Sensor," *IEEE Symp. VLSI Circuits Dig. of Tech. Papers*, pp. 137 – 138.
- [14] S. Kleinfelder, S. Lim, X. Liu and A. E. Gamal. 2001. "A 10k frame/s 0.18 μm CMOS Digital Pixel Sensor with Pixel-Level Memory," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 88 – 89.
- [15] V. Brajovic, K. Mori and N. Jankovic. 2001. "100 frames/s CMOS Range Image Sensor," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 256 – 257.
- [16] S. Yoshimura, T. Sugiyama, K. Yonemoto and K. Ueda. 2001. "A 48k frame/s CMOS Image Sensor for Real-time 3-D Sensing and Motion Detection," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 94 – 95.
- [17] T. Sugiyama, S. Yoshimura, R. Suzuki and H. Sumi. 2002. "A 1/4-inch QVGA Color Imaging and 3-D Sensing CMOS Sensor with Analog Frame Memory," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 434 – 435.
- [18] T. Nezuka, M. Hoshino, M. Ikeda and K. Asada. 2000. "A Position Detection Sensor for 3-D Measurement," in *Proc. of European Solid-State Circuits Conference (ESSCIRC)*, pp. 412 – 415.
- [19] Y. Oike, M. Ikeda and K. Asada. 2003. "High-Speed Position Detector Using New Row-Parallel Architecture for Fast Collision Prevention System," in *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 4, pp. 788 – 791.
- [20] Y. Oike, M. Ikeda and K. Asada. 2004. "A 375 x 365 3D 1k frame/s Range-Finding Image Sensor with 394.5 kHz Access Rate and 0.2 Sub-Pixel Accuracy," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*.
- [21] T. Nezuka, M. Ikeda and K. Asada. 2002. "A Smart Position Sensor With Row Parallel Position Detection for High Speed 3-D Measurement," in *Proc. of European Solid-State Circuits Conference (ESSCIRC)*, pp. 101 – 104.
- [22] Y. Oike, M. Ikeda and K. Asada. 2003. "A CMOS Image Sensor for High-Speed Active Range Finding Using Column-Parallel Time-Domain ADC and Position Encoder," *IEEE Trans. on Electron Devices*, vol. 50, no. 1, pp. 152 – 158.
- [23] Y. Oike, M. Ikeda and K. Asada. 2003. "640 x 480 Real-Time Range Finder Using High-Speed Readout Scheme and Column-Parallel Position Detector," *IEEE Symp. VLSI Circuits Dig. of Tech. Papers*, pp. 153 – 156.
- [24] T. Chen, P. Catrysse, A. E. Gamal and B. Wandell. 2000. "How Small Should Pixel Size Be?" in *Proc. of SPIE*, vol. 3965, pp. 451 – 459.

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