A Smart Image Sensor With High-Speed Feeble ID-Beacon Detection for Augmented Reality System

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Abstract

In this paper, we present a smart image sensor with high-speed feeble ID-beacon detection for an augmented reality (AR) system. AR systems are designed to provide an enhanced view of the real world with meaningful information from a computer. Our target AR system uses an optical device with ID beacon such as a blinking LED. Our sensor architecture realizes analog readout for 2-D image capture and high-speed digital readout for ID beacon detection simultaneously. The pixel circuit has a logarithmic-response photo detector and an adaptive modulation amplifier to detect a feeble ID beacon in wide range of background illumination. A 128 × 128 smart sensor has been developed and successfully tested. It achieves 4850 bit/ID·sec using 40 kHz carrier and < -10.0 dB signal-to-background ratio (SBR) in > 40 dB background illumination for robust ID-beacon detection.

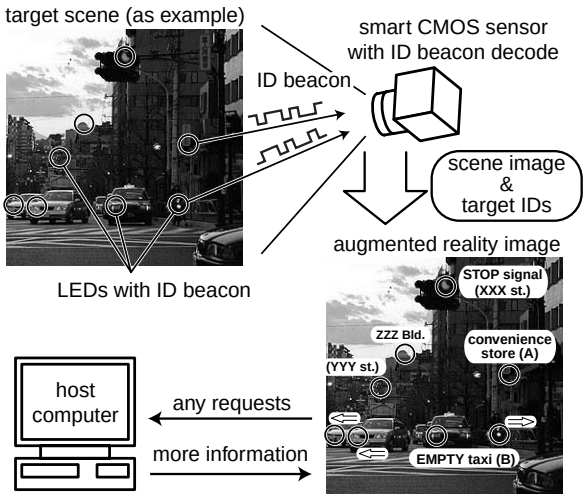

Figure 1. An Example of Augmented Reality System

1. Introduction

In recent years, our real world becomes closely tied to a computer world due to wide use of PDA and its network infrastructure. Then an augmented reality (AR) system becomes important as an interface between the real world and the computer world. In the AR system, the information of the computer world is attached to a view of the real world to support human activities. Some methods have been proposed for such an AR system up to now. In a visual tagging system[1], a 2-D barcode with ID is attached to a target object and captured by a barcode reader. An AR system using RF-ID tags[2] also requires an ID reader. Therefore it is difficult for these methods to get both the locations and IDs of some target objects. An AR system using optical devices with an ID beacon[3] is a possible solution to the problem. It can get a scene image, locations and IDs of one or more target objects simultaneously as shown in Fig.1. It, however, limits a carrier speed of ID beacon due to a standard image sensor of 30 fps. Its data rate using 15 Hz carrier is not enough to identify a lot of moving objects. An AR system[4] using a high-speed smart image sensor[5] achieves 120 bit/ID·sec data rate using 4 kHz carrier and packet transmission. It corresponds to 8-bit ID detection in 15 fps. Yet it is not enough to identify various objects in the real world.

Our present smart image sensor realizes high-speed feeble ID-beacon detection and provides the next step for a practical AR system. Our digital readout scheme and circuits utilize a high-speed carrier of ID beacon to transfer a lot of information in real time and to identify various objects in the real world. In addition, the pixel circuit with a logarithmic-response photo detector and an adaptive modulation amplifier allows the feeble ID-beacon detection for both indoor and outdoor applications. The adaptive sensing and high-speed readout scheme also contributes to asynchronous system among a sensor and ID beacons. A 128 × 128 smart image sensor has been developed using 0.35 μm CMOS process and successfully tested.

2. Sensor Architecture

Our present sensor consists of a pixel array with an adaptive modulation amplifier, two row-select decoders, source follower readout circuits with a column selector, column-parallel dynamic logics with a sense amplifier for digital readout, and a multiplexer with output buffers as shown in Fig.2. In a pixel, an feeble incident light from ID beacon is amplified by logarithmic-response and adaptive constant-illumination suppression to realize high-sensitivity beacon detection in wide range of background illumination. When the pixel is selected, the amplified beacon signals are digitized by a column-parallel dynamic logic with a sense amplifier and an in-pixel thresholding readout circuit. Our digital readout scheme achieves high-speed beacon sampling and feeble beacon detection by compact circuit implementation.

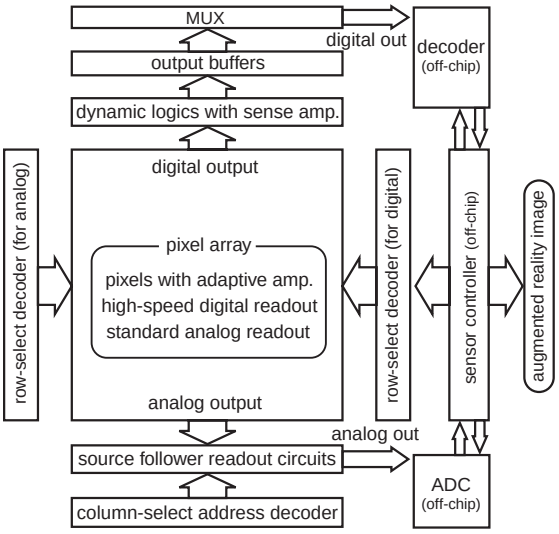

Figure 2. Block Diagram of the Smart Sensor

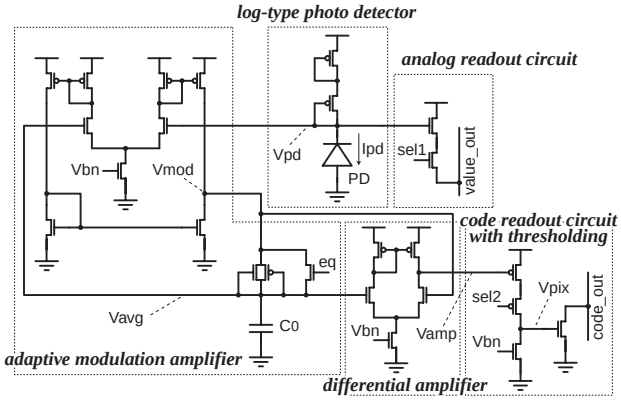

Figure 3. Pixel Circuit Configuration

In addition, the digital beacon readout operates independently of analog readout for 2-D image. A beacon decoder, an ADC for 2-D image and a sensor controller in Fig.2 are implemented in an FPGA, not integrated in our prototype sensor.

3. Circuit Configuration

3.1. Pixel Circuit and Operation

Fig.3 shows our pixel circuit with an adaptive modulation amplifier and analog/digital readout circuits. An incident light generates Vpd in logarithmic response to its intensity. The logarithmic-response photo detector contributes to avoid a saturation problem for wide range of background illumination and to keep asynchronous among a reset cycle and ID beacons. The analog signal Vpd for 2-D image is read out by a source follower circuit via a column line *value_out* . The log-response 2-D image is not high quality but enough and suitable for an AR system to recognize what kind of objects in a non-uniform contrast scene.

On the other hand, Vpd is fed into an adaptive modulation amplifier. At the adaptive modulation amplifier, the average level $Vavg$ is generated and subtracted from the original Vpd for a feeble ID-beacon detection in wide

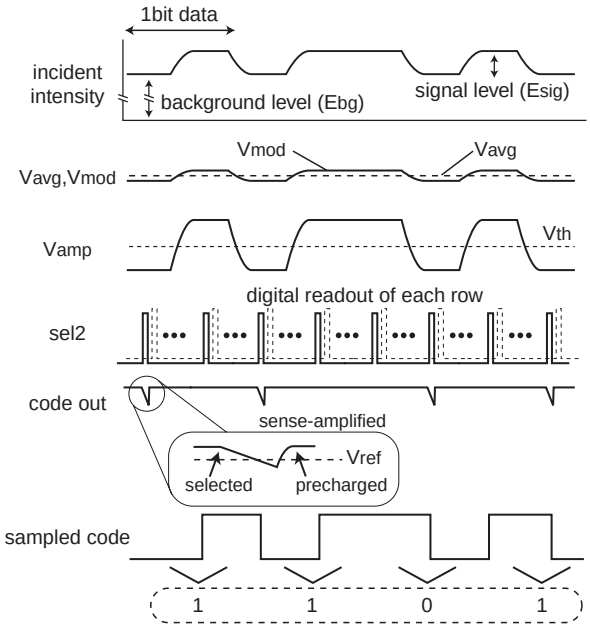

Figure 4. Timing Diagram of the Pixel

range of background illumination. The output swing of $Vmod$ is amplified again by a differential amplifier with the adaptive reference voltage $Vavg$. At a code readout circuit with thresholding, $Vpix$ of a non-selected pixel is set to low level. After a pixel is selected by *sel*2, the voltage level of $Vpix$ is decided by compared with a bias voltage Vbn. A precharged line *code_out* is changed in accordance with $Vpix$. A column-parallel sense amplifier digitizes an ID-beacon signal of a selected pixel.

Fig.4 shows a timing diagram of our pixel circuits. In an AR system using active optical devices, an incident light can contain a beacon signal $Esig$ as well as background illumination Ebg. We assume the background illumination is generally constant or low frequency below 100 Hz. When an incident light has a beacon signal, our pixel circuits amplify only the beacon signal and generate $Vamp$ due to adaptive constant-illumination suppression. The adaptive suppression requires the average level $Vavg$ of $Esig + Ebg$. Therefore 1-bit data of a target ID is coded using 2 cycles of carrier to keep 50% duty. That is, '01' and '10' represent '1' and '0' respectively. This coding is the same as [4] using a special image sensor [5], which detects only a positive edge of an incident level.

3.2. Analog/Digital Readout Circuit

To utilize a high-speed ID-beacon carrier, high-speed frame readout is required. Column-parallel dynamic logics with a sense amplifier achieve high-speed sampling and digitization of $Vpix$ as shown in Fig.5. First, an output *code_out* is set to high level by *pre*. Then the voltage level of *code_out* is compared with $Vref$ and digitized by a sense amplifier at a positive edge of *sck* shortly after a pixel is selected by *sel*2. Finally the results of digital frame readout are transferred to output buffers by *ock* and sent to an off-chip decoder every 32 bits within the next readout cycle. The readout clock cycle achieves 200 MHz in a circuit simulation of our 128×128 prototype sensor.

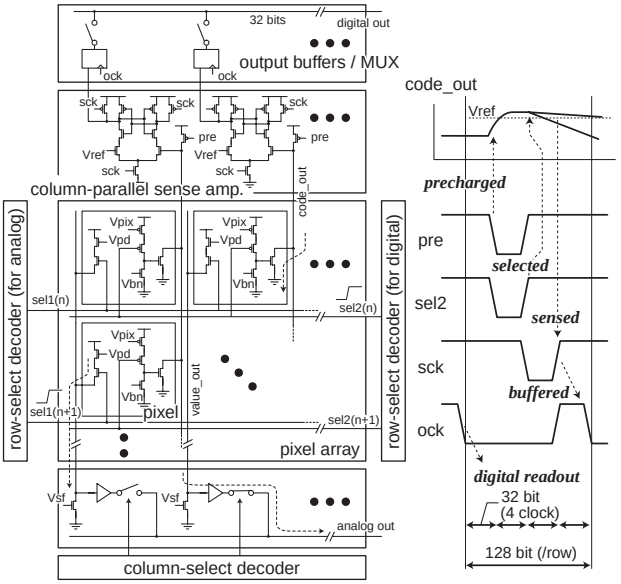

Figure 5. Analog/Digital Readout Circuit and Operation

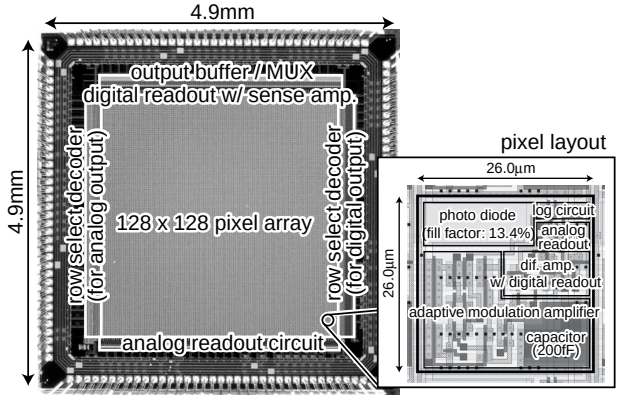

Figure 6. Chip Microphotograph and Pixel Layout

Supposing that the digital frame rate requires ×4 of carrier speed to sample asynchronous beacon data without fault, it utilizes 100 kHz ID-beacon carrier.

4. Chip Implementation

We designed and fabricated a smart sensor using the present pixel circuit in 0.35 μm CMOS process[1]. Fig.6 shows a microphotograph of the fabricated smart sensor. It has a 128 × 128 pixel array with independent analog/digital readout circuits. The pixel circuit occupies 26.0μm × 26.0μm with 13.4% fill factor. The pixel layout is also shown in Fig.6. The photo diode is formed by an n^+-diffusion in a p-substrate. The in-pixel capacitance of C_0 in Fig.3 is 200 fF. The parameters of the fabricated sensor are summarized in Table 1. The power dissipation is 682 mW at 40MHz, 4.2 V power supply. Our pixel circuits are more suitable for high pixel resolution than the conventional special smart sensor [5] since the pixel size is about 1/4 of [5].

[1]The sensor in this study has been fabricated through VLSI Design and Education Center (VDEC), University of Tokyo in collaboration with Rohm Co. and Toppan Printing Co.

Table 1. Parameters of the Fabricated Sensor

Process	0.35 μm CMOS 3-metal 1-poly-Si
Chip size	4.9 mm × 4.9 mm
# pixels	128 × 128 pixels
Pixel size	26.0 μm × 26.0 μm
Fill factor	13.4 %
Power Dissipation	682 mW (@40MHz, 4.2V)

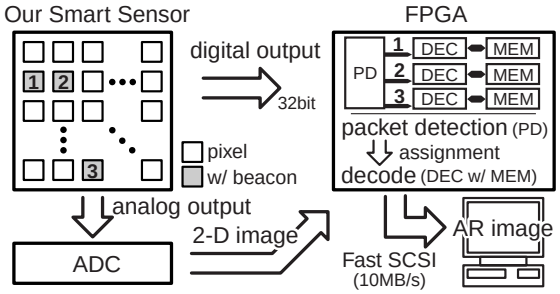

Figure 7. Measurement System Structure

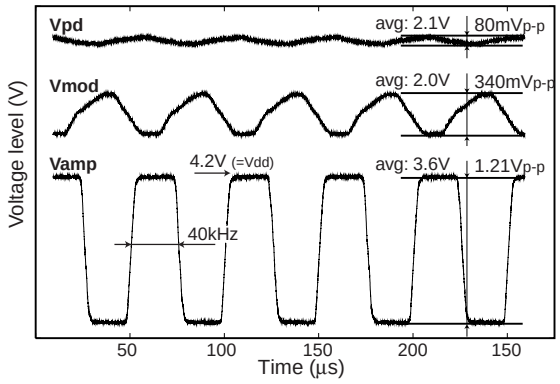

Figure 8. Measured Waveforms

5. Measurement Results

Fig.7 shows a measurement system of the fabricated sensor. It consists of our smart sensor with a lens, an external ADC, an FPGA and a host computer. Our FPGA operates 40 MHz, which employs sensor control, ID decode and data transmission. A red LED of 620 nm wave length is used for a target ID beacon. Fig.8 shows measured waveforms of *Vpd*, *Vmod* and *Vamp* in Fig.3 when a beacon carrier speed is 40 kHz. Our pixel circuits amplify *Vpd* adaptively and generate *Vamp* for digital readout.

5.1. Frame Rate with ID-Beacon Detection

Our sensor has independent frame rates of analog and digital readout as mentioned previously. The analog frame rate is 30 fps in our measurement, which is limited by an external ADC. It is enough for a real-time AR system. If the pixel resolution becomes higher, it will require a high-speed ADC or a column-parallel ADC to keep 30 fps of 2-D image capture. The digital frame rate should be adapted to ID-beacon carrier. Therefore we set the frame rate to ×4 of carrier speed to sample an ID beacon without fault. In the measurement system, an ID beacon using 40 kHz carrier was successfully sampled. We applied

Table 2. Performance Comparison

	# pixels	pixel size	carrier	data bandwidth	AR images/s
A Standard CCD Imager [3]	N/A	N/A	15 Hz	6 bit/ID·sec	0.2 fps
Yoshimura, ISSCC'01 [4, 5]	192×124	$^{\dagger}46.4 \times 54.0\ \mu m^2$	4 kHz	120 bit/ID·sec	15 fps
Our Present Smart Imager	$\mathbf{128 \times 128}$	$^{\dagger}\mathbf{26.0 \times 26.0}\ \mu m^2$	**40 kHz**	**4850 bit/ID·sec**	**30 fps**

†Both of them are fabricated in 0.35 μm process

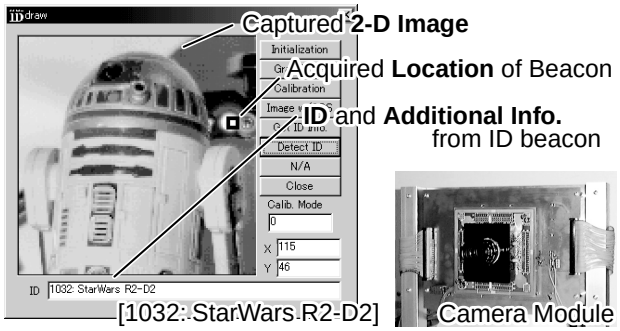

Figure 9. Reproduced Image with ID Information

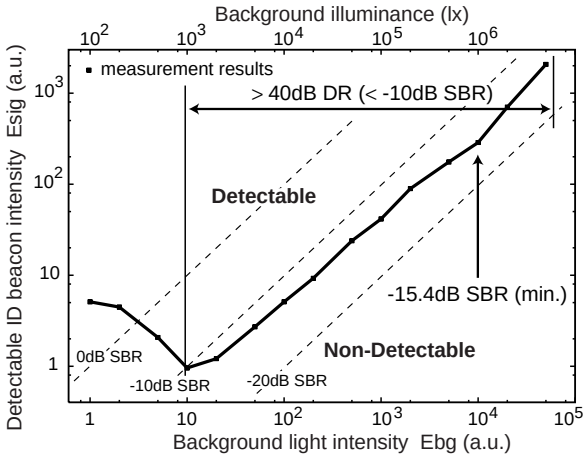

Figure 10. Sensitivity and Dynamic Range of ID-Beacon Detection

packet transmission to our measurement system for asynchronous ID-beacon sampling. A packet consists of 4-bit header, 16-bit coded data and 2-bit footer to transfer 8-bit data for ID. In addition, a packet sequence of ID beacon is repeated 3 times in one frame of AR images. This packet protocol is based on [4]. In this situation, the data bandwidth is 4850 bit/ID·sec, which provides 160-bit data for each target ID in 30 fps. Our proposed scheme has more potential of high-speed sampling since it is limited by the sensor control speed by an FPGA and the photo sensitivity of a standard digital CMOS process. Fig.9 shows a reproduced image with ID information from a blinking LED. It has additional information of the target object as well as its ID number due to large capacity of bandwidth.

5.2. Sensitivity and Dynamic Range

Fig.10 shows the sensitivity and dynamic range of ID-beacon detection. Our pixel circuit can detect a feeble incident swing of ID beacon in wide range of background illumination. The minimum detectable intensity of ID beacon is measured using TEGs of a pixel circuit. To evaluate the sensitivity of the photo detection, the ID-beacon intensity and the background intensity are normalized by the photo current I_{pd} of each incident light. The illuminance corresponding to the background photo current is shown in Fig.10 (in the upper axis) for reference. We define $10 \log E_{sig}/E_{bg}$ as SBR (Signal-to-Background Ratio), which stands for the sensitivity of beacon detection. High sensitivity below -10.0 dB SBR is achieved in wide range of > 40 dB background illumination.

5.3. Performance Comparison

The performance comparison is summarized in Table 2. The AR system using a 30-fps CCD imager provides 0.2 AR images/sec with 16 IDs/frame [3]. Even the state-of-the-art high-speed CMOS imager [6], which achieves 10k fps imaging, utilizes only 2.5 kHz beacon carrier. The AR system [4] using a special image sensor [5] allows 4 kHz beacon carrier. It, however, has the capability to recognize only 8-bit IDs/frame in 15 fps. Our present smart sensor utilizes 40 kHz carrier and recognizes 160-bit IDs/frame in 30 fps in the same situation. The large capacity of bandwidth has a potential to attach additional and meaningful information to an AR image from the target objects.

6. Conclusions

Our 128×128 smart sensor achieves 30-fps scene capture, 4850 bit/ID·sec using 40 kHz carrier, and < -10.0 dB signal-to-background ratio (SBR) in > 40 dB background illumination for a high-speed and robust AR system with active optical devices. It enables to get a scene image, locations, IDs and additional information of multiple target objects simultaneously in real time. The advanced performance provides the next step for a practical AR system.

7. References

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