6.6 A 375 x 365 3D 1k frame/s Range-Finding Image Sensor with 394.5 kHz Access Rate and 0.2 Sub-Pixel Accuracy

Y. Oike, M. Ikeda, K. Asada

University of Tokyo, Tokyo, Japan

High-speed and high-resolution 3-D imaging has a wide variety of applications including gesture recognition, security systems, computer vision, movies and televisions. Moreover ultra-high-speed range finding provides the possibility of additional applications such as quick inspection of industrial components, a fast visual feedback in robot vision and the observation of structural deformation and destruction. A light-section 3-D measurement provides a high-accuracy 3-D image. However reconstruction of a range map by triangulation requires the detection of many positions of a scanning sheet beam on the sensor plane. State-of-the-art sensors based on the light-section method [1]–[4] are reported for real-time 3-D imaging systems of 15 -100frames/s. It is difficult for these sensors to realize 3-D measurements with practical resolution for range-finding over 1,000frames/s. A row-parallel search architecture is reported with a potential capability of 1,000frames/s range finding with a practical resolution [5]. This paper presents a 3-D image sensor with 375x365 pixels for 1,000frames/s range finding based on the light-section method. The row-parallel search architecture is implemented with a new multi-sampling function for a fine sub-pixel resolution using a standard 0.18μm CMOS process.

Figure 6.6.1 is a block diagram illustrating the 3-D image sensor with the row-parallel search architecture. It consists of a pixel array, bit-streamed column address generators, row-parallel processors with 18b registers and output buffers, and an on-chip controller with a PLL. Additionally a row scanner and a multiplexer are used for the conventional 2-D imaging. In the row-parallel search architecture, several ideas are employed. The left and right edges of consecutively activated pixels are detected alternately by a search signal propagation via chained search circuits in row parallel. It enables positions of the incident sheet beam to be detected quickly regardless of the number of the activated pixels in row.

A row-parallel acquisition of column addresses of detected pixels is realized by column-parallel address streaming. The column address streams are injected at the top of the sensor vertically and change their direction horizontally at pixels detected by the search circuits. It achieves O(log N) acquisition cycles by a compact circuit of 2 FETs in each pixel in a case of a sensor with NxN pixels.

Row-parallel processors receive the bit-streamed column address and calculate the center position of activated pixels during address acquisition. It achieves a high-speed address acquisition and a multi-sampling method. The multi-sampling method provides the intensity profile of incident beam to improve the sub-pixel resolution. The row-parallel processors carry out pre-processing for center position calculation to reduce the data transmission.

Figure 6.6.2 shows circuit configurations of a pixel and a row-parallel processor and Fig. 6.6.3 shows their timing diagram. After photo current integration started with RST, V_{pd} is converted to digital data and latched by CK as the pixel value. Here pixels with strong incident intensity are activated. Vb controls its threshold level and suppresses the short-circuit current. To detect the left edge of activated pixels, LSW is set to high and RSW is set to low. The first search trigger SCH_0 is set to low to clear the search signal propagation path (SCH_1, SCH_2, ...SCH_n). To initiate the search operation, SCH_0 is set to high in row parallel. The high level at SCH_i is transferred to the next pixel at SCH_{i+1} so far as the pixels are inactivated. It stops at the first-detected activated pixel (i.e. left edge) as indicated by SCH_l in Fig. 6.6.3. The column address line and the row address line are connected at the detected pixel, and the bit-streamed column address ADDj is transferred from the column line to the row line. It is received and stored by a row-parallel processor. After the address acquisition, all pixel values are inverted by LSW=0 and RSW=1. The search signal SCH_l restarts from the left edge and skips activated pixels up to the next of the right activated pixel. Then the address acquisition is carried out in the same way. The right address is added to the left address by the row-parallel processor while the address acquisition. The row-parallel processor can accumulate the detected pixel positions and count the number of samplings in order to calculate fine sub-pixel positions in post-processing. The accumulated data are transferred to output buffers by TR.

The 3-D image sensor of Fig. 6.6.4 is a 375x365 pixel array and is designed and fabricated in a 0.18μm 1P5M CMOS process. The pixel area is 11.25x11.25μm^2 with 24 FETs and 22.8% fill factor as shown in Fig. 6.6.4. The clock signal of an on-chip controller is generated by a PLL (x8/x16, 300~550MHz). The on-chip controller has a test mode to evaluate the worst-case access rate, where test image patterns are generated electrically on the sensor plane.

Figure 6.6.5 displays the cycle times of the activated pixel search and the data readout with a 400MHz clock. The pixel activation by the incident beam, the activated pixel search with the column address acquisition, and the data readout from the output buffers are carried out at the same time in a pipelined mode. The pixel activation time depends on the beam intensity and can be reduced by a sharp and strong projected sheet beam. The limiting factor of access rate is data readout from the output buffers. The multi-sampling operation can be carried out four times during the previous data readout. The worst-case test by the on-chip controller shows the maximum access rate of 394.5kHz at 432MHz and it corresponds to 1052 range maps/s with 375x365 range data. Moreover the multi-sampling method achieves 0.2 sub-pixel resolution of position detection. The measurement result shows that the maximum range error is 1.10mm and the standard deviation of error is 0.47mm at 600mm distance. Figure 6.6.6 shows an example of measured range data of a target object placed at 600mm from the sensor with a lens. The characteristics of the present sensor are summarized in Fig. 6.6.7

Acknowledgements:
The chip was fabricated by the VLSI Design and Education Center, Univ. of Tokyo, in collaboration with Hitachi Ltd. and Dai Nippon Printing Co.

References:
[1] V. Brajovic et al., "100Frames/s CMOS Range Image Sensor," *ISSCC Dig. Tech. Papers*, pp. 256–257, Feb. 2001.
[2] S. Yoshimura et al., "A 48k Frame/s CMOS Image Sensor for Real-Time 3-D Sensing and Motion Detection," *ISSCC Dig. Tech. Papers*, pp. 94–95, Feb. 2001.
[3] T. Sugiyama et al., "A 1/4-inch QVGA Color Imaging and 3-D Sensing CMOS Sensor with Analog Frame Memory," *ISSCC Dig. Tech. Papers*, pp. 434–435, Feb. 2002.
[4] Y. Oike et al., "640x480 Real-Time Range Finder Using High-Speed Readout Scheme and Column-Parallel Position Detector," *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 153–156, June, 2003.
[5] Y. Oike et al., "High-Speed Position Detector Using New Row-Parallel Architecture for Fast Collision Prevention System," *Proc. of Int. Symp. Circuits and Systems*, pp. 788–791, May, 2003.

 0-7803-8267-6/04

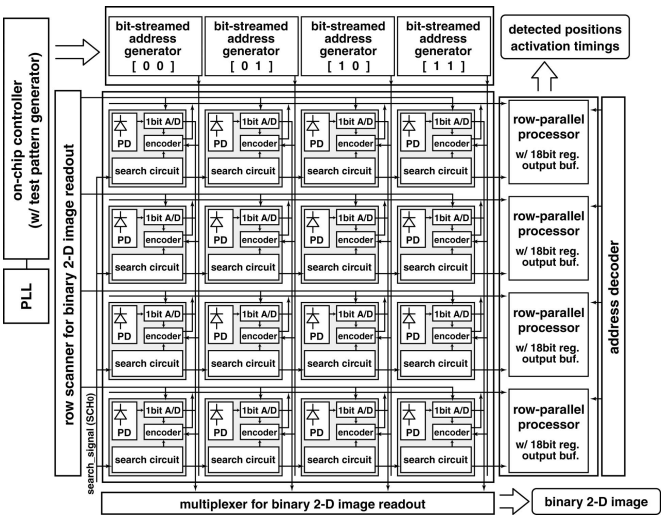

Figure 6.6.1: Simplified block diagram of 4.4 pixels. (The designed chip has an array of 375 x 365 pixels.)

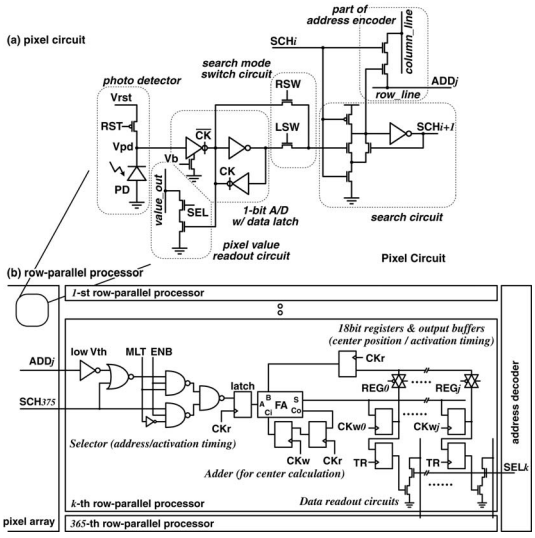

Figure 6.6.2: Circuit configuration: (a) pixel circuit, (b) row-parallel processor.

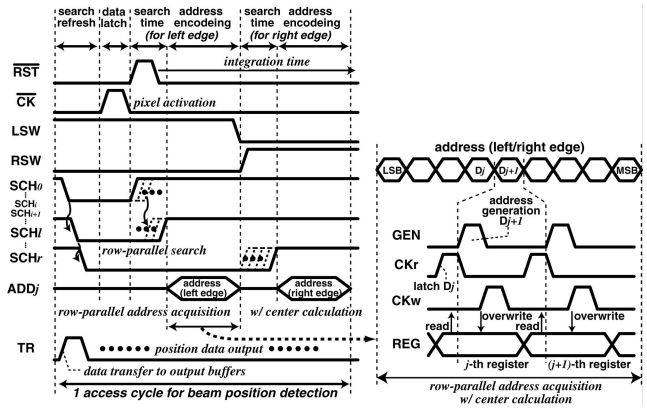

Figure 6.6.3: Timing diagram.

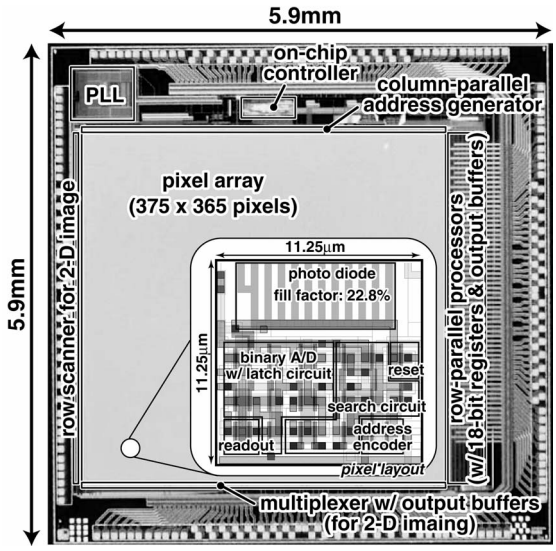

Figure 6.6.4: Die microphotograph and pixel layout.

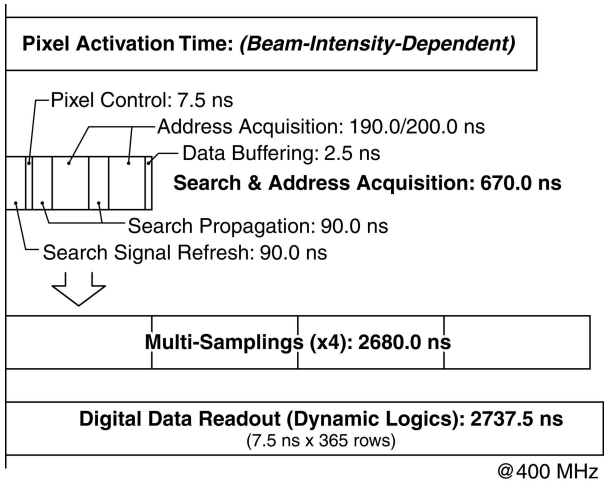

Figure 6.6.5: Cycle times of activated pixel search and data readout.

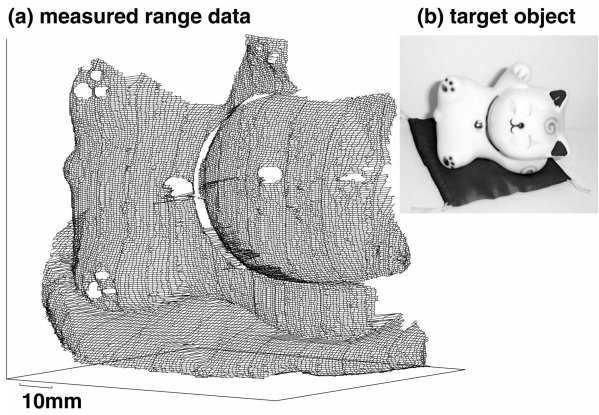

Figure 6.6.6: Measurement result of range finding.

 0-7803-8267-6/04

Process	0.18μm CMOS 5-metal 1-poly-Si
Chip Size	5.9 mm x 5.9 mm
# Pixels	375 x 365 pixels
Pixel Size	11.25 μm x 11.25 μm
Fill Factor	22.8 %
# FETs/Pixel	24 FETs/pixel
# Total FETs	3.74 M FETs
Supply Voltage	1.8V
Max. Clock Freq.	432 MHz
Access Rate	394.5 kHz
Data Rate	144M bit/pin.sec
Range Finding Speed	1052 range maps/sec
Sub-Pixel Resolution	0.2 pixels
Range Accuracy	max. 1.10 mm @ 600 mm
	SD 0.47 mm @ 600 mm
Power Dissipation	1065 mW (@432MHz, 1.8V)

Figure 6.6.7: Chip specification.

0-7803-8267-6/04

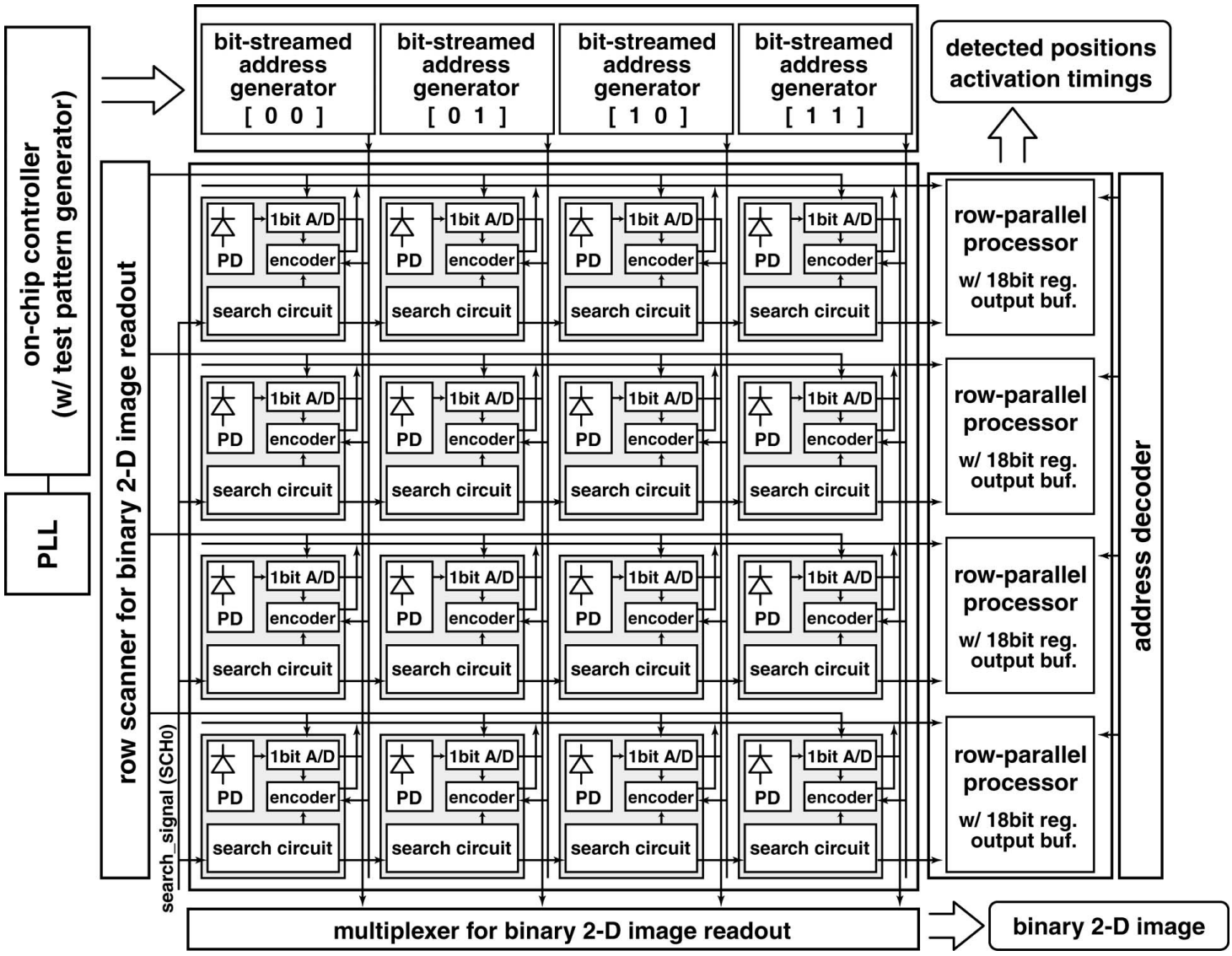

Figure 6.6.1: Simplified block diagram of 4.4 pixels. (The designed chip has an array of 375 x 365 pixels.)

0-7803-8267-6/04

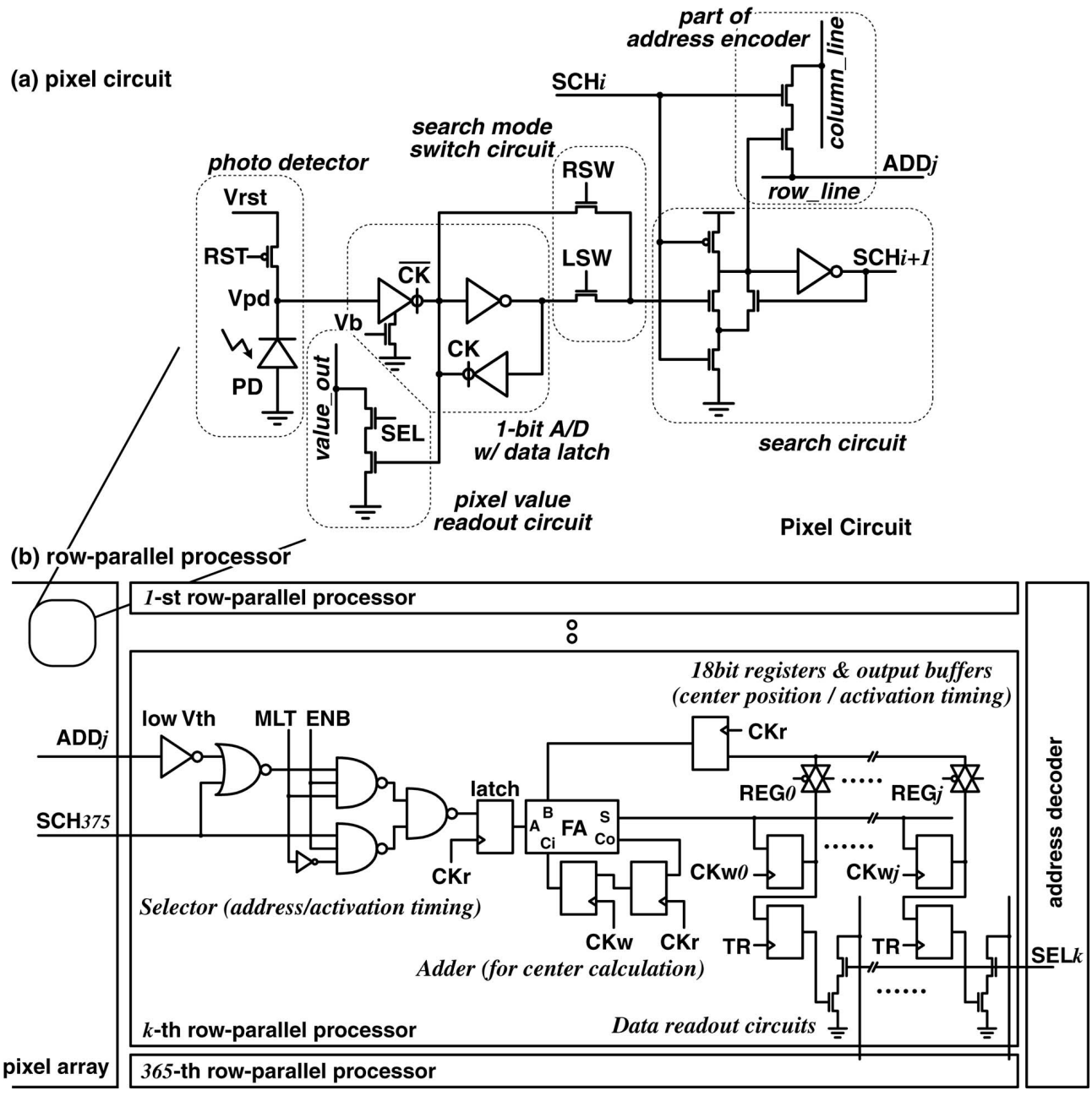

Figure 6.6.2: Circuit configuration: (a) pixel circuit, (b) row-parallel processor.

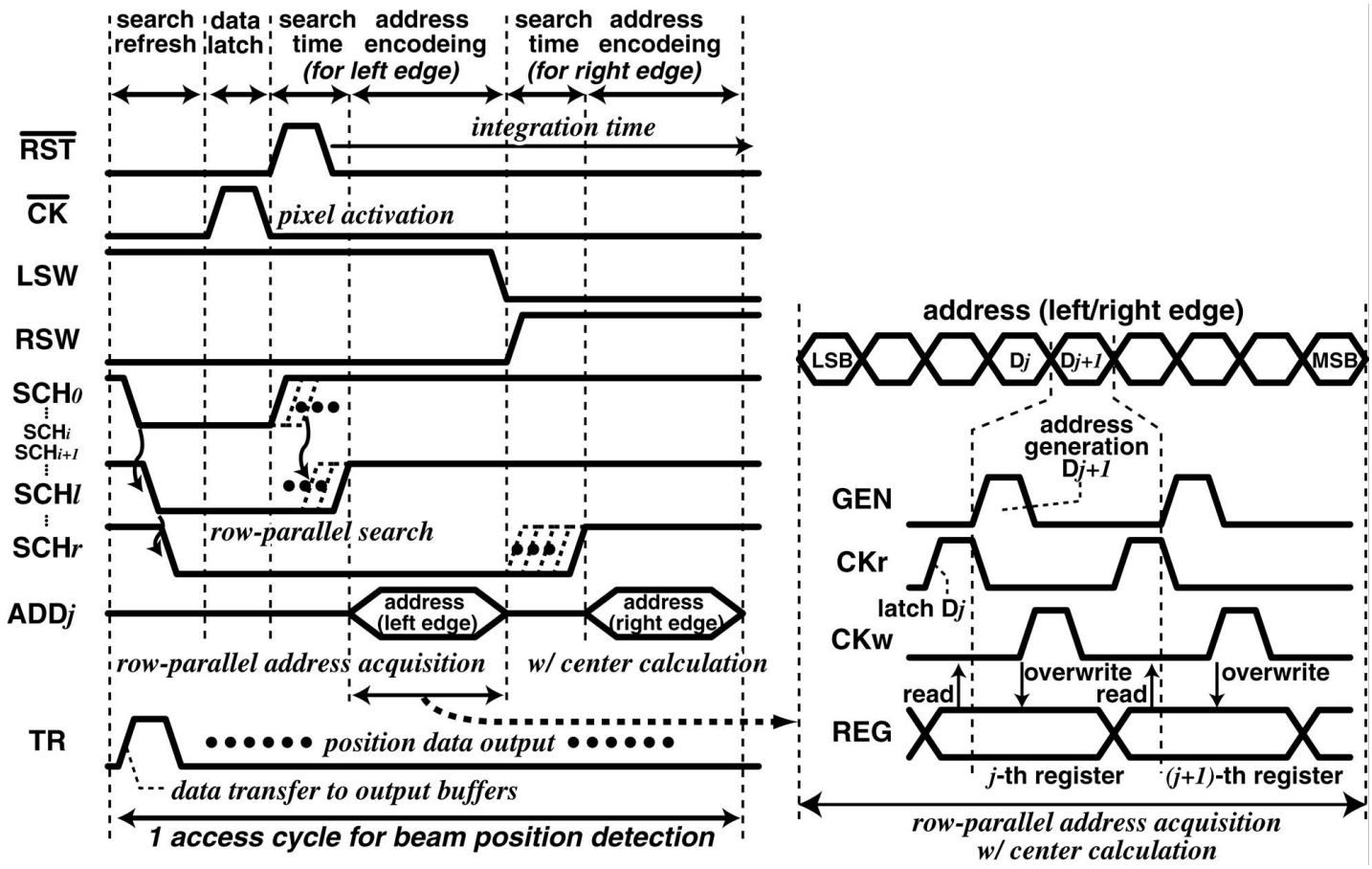

Figure 6.6.3: Timing diagram.

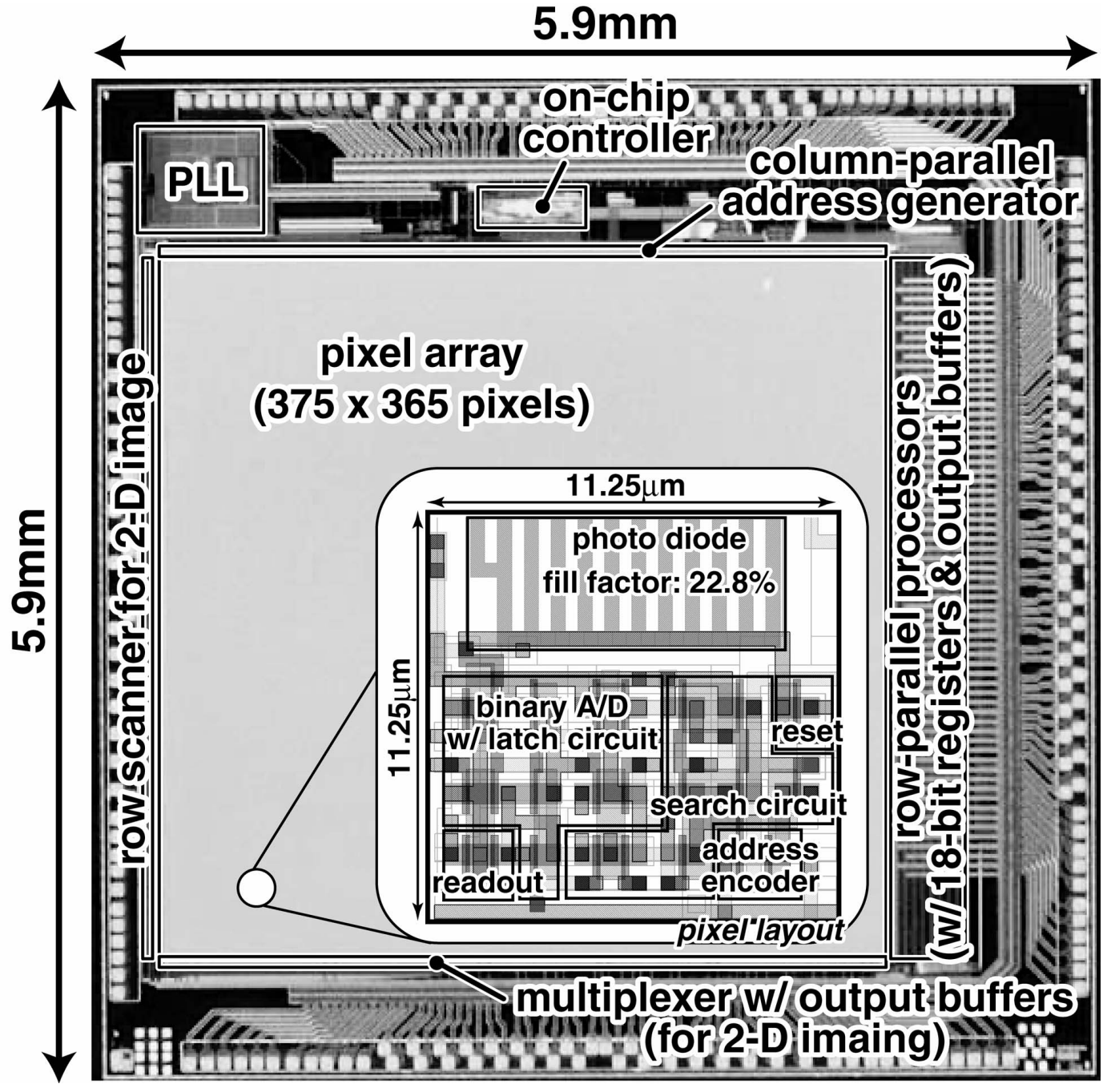

Figure 6.6.4: Die microphotograph and pixel layout.

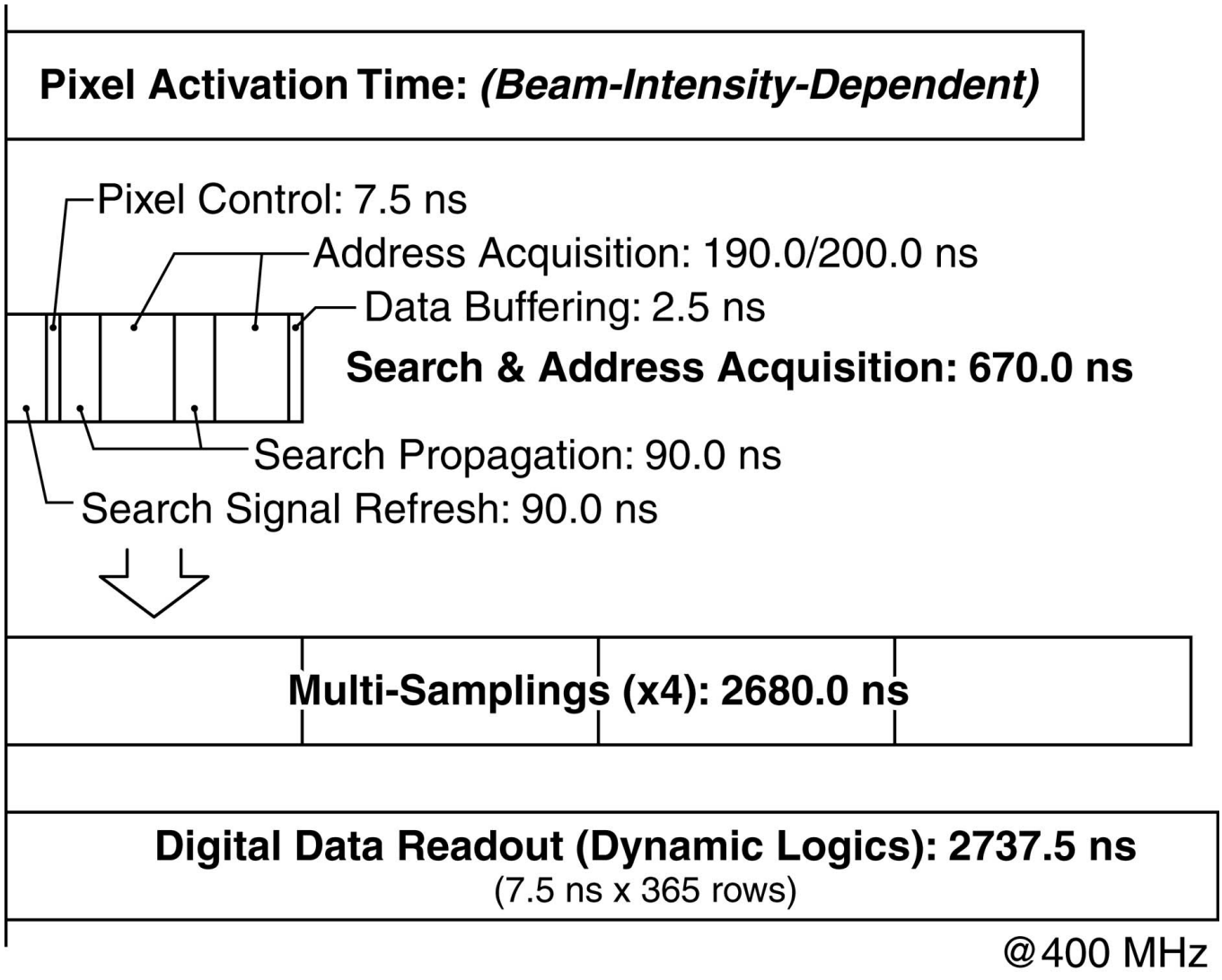

Figure 6.6.5: Cycle times of activated pixel search and data readout.

0-7803-8267-6/04

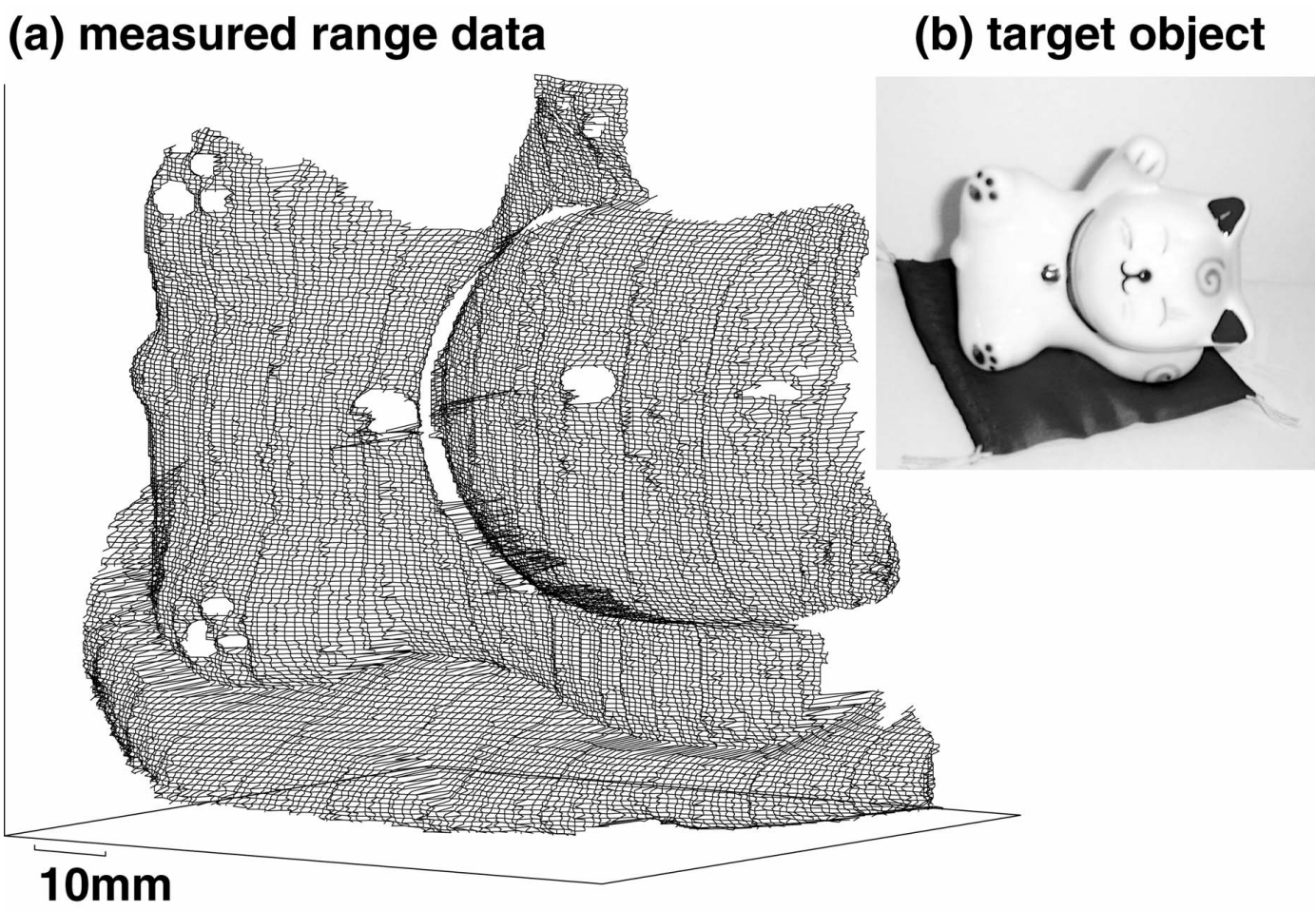

Figure 6.6.6: Measurement result of range finding.

Process	0.18μm CMOS 5-metal 1-poly-Si
Chip Size	5.9 mm x 5.9 mm
# Pixels	375 x 365 pixels
Pixel Size	11.25 μm x 11.25 μm
Fill Factor	22.8 %
# FETs/Pixel	24 FETs/pixel
# Total FETs	3.74 M FETs
Supply Voltage	1.8V
Max. Clock Freq.	432 MHz
Access Rate	394.5 kHz
Data Rate	144M bit/pin.sec
Range Finding Speed	1052 range maps/sec
Sub-Pixel Resolution	0.2 pixels
Range Accuracy	max. 1.10 mm @ 600 mm
	SD 0.47 mm @ 600 mm
Power Dissipation	1065 mW (@432MHz, 1.8V)

Figure 6.6.7: Chip specification.

0-7803-8267-6/04