Design and Implementation of Real-Time 3-D Image Sensor With 640 × 480 Pixel Resolution

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***Abstract*—In this paper, the first real-time range finder with the capability of VGA (640 × 480) resolution based on the light-section method is presented. We propose an adaptive thresholding circuit and column-parallel time-domain approximate analog-to-digital converters to realize high-speed readout for real-time range finding. Sub-pixel position calculation based on intensity profile achieves high-accuracy range finding. A column-parallel position detector suppresses redundant data transmission for a real-time measurement system. A 640 × 480 range finder using these techniques has been developed and successfully tested. The maximum range finding speed is 65.1 range_maps/s. The maximum range error is 0.87 mm and the standard deviation of error is 0.26 mm at 1200-mm distance. We have acquired a two-dimensional image and a high-resolution three-dimensional (3-D) image by the 3-D measurement system using our range finder.**

***Index Terms*—High resolution, light-section method, position sensor, range finding, real time, three-dimensional image sensor, VGA.**

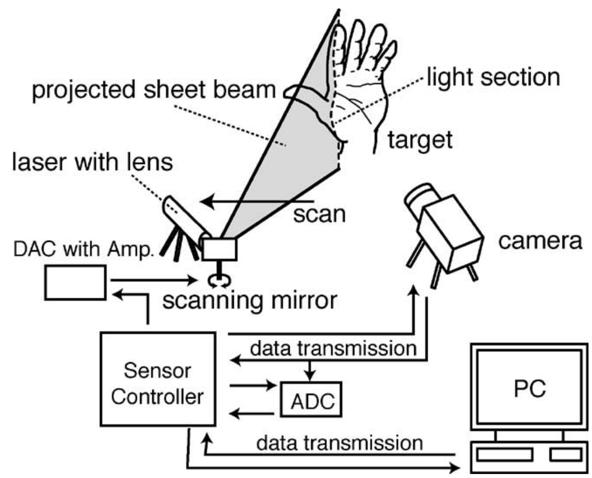

Fig. 1. 3-D measurement system based on the light-section method.

I. Introduction

In recent years, we have often seen three-dimensional (3-D) computer graphics in movies and televisions, and handled them interactively using personal computers and video game machines. The latest and future 3-D applications require both higher pixel resolution for accurate range finding and higher frame rate for real time. Fig. 1 shows a structure of 3-D measurement system based on the light-section method, which is a typical range finding method, the same as the stereo-matching method and the time-of-flight method. The system based on the light-section method allows highly accurate range finding by simple triangular calculation. However, it requires thousands of images every second for real-time 3-D measurement. For example, a 1024 × 1024 range map in video rate needs 30 kfps. This is difficult for a standard readout architecture such as CCD. Even the high-speed CMOS active pixel sensor (APS) using column-parallel analog-to-digital converters (ADCs) [1] realizes 500 fps at most. Some position sensors for fast range finding have been reported in [2]–[4]. A range finder using a row-parallel winner-take-all (WTA) circuit [2] realizes 100 range_map/s with 64 × 64 range data. A 3-D image sensor using a pixel-parallel architecture [3] can acquire a 192 × 124 range map in video rate. A 320 × 240 (QVGA) color imager with analog frame memories out of a pixel array [4] achieves 160 × 120 3-D imaging in 15 range_maps/s. However, it is difficult for them to get a 3-D image in real time with higher pixel resolution.

In this paper, we present the first real-time range finder with the capability of VGA (640 × 480) resolution based on the light-section method. We propose two techniques for high-resolution and real-time range finding: a high-speed readout scheme and a column-parallel position detector. The high-speed readout scheme using adaptive thresholding and time-domain approximate ADCs achieves high frame rate for real-time range finding and high range accuracy due to sub-pixel position calculation. A 128 × 128 prototype sensor using our basic idea [5] shows that it has a potential for real-time range finding with very high pixel resolution such as VGA or more.

Now, a 640 × 480 range finder using these techniques has been developed and successfully tested. In Section II, our sensing scheme and sensor architecture are presented. In Section III, circuit configurations and operations are described. In Section IV, the chip implementation and specification of our 3-D image sensor are shown. In Section V, the performance and measurement results of the fabricated sensor are shown. Finally, conclusions are presented in Section VI.

II. Sensing Scheme and Sensor Architecture

Fig. 2 shows the proposed sensing procedure for high-speed position detection. In the range finding, an image sensor receives a scene image and a reflection of a projected sheet beam. For two-dimensional (2-D) imaging, all pixels are accessed using a raster scan to read out the pixel values. On the other hand, the position of the projected sheet beam on the sensor plane is needed for range finding. Therefore, a row

Manuscript received July 4, 2003; revised October 9, 2003.

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Digital Object Identifier 10.1109/JSSC.2004.825122

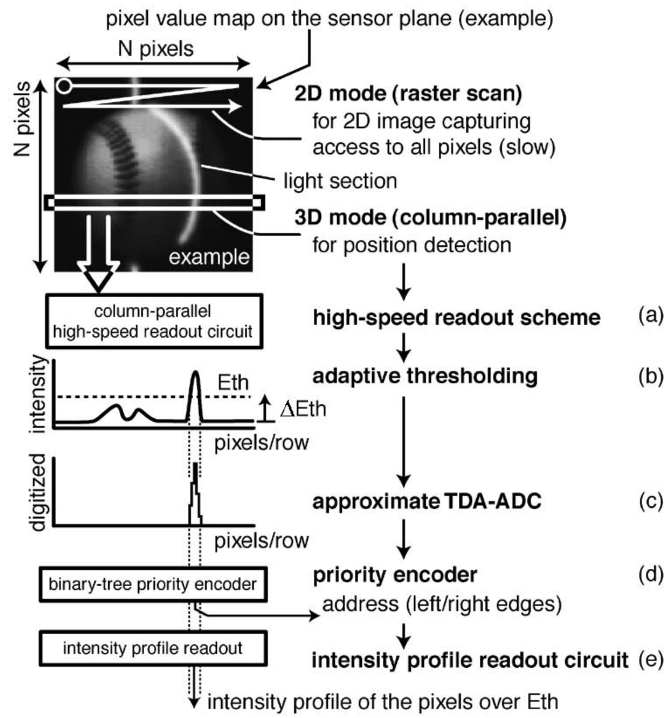

Fig. 2. Sensing procedure for high-speed position detection.

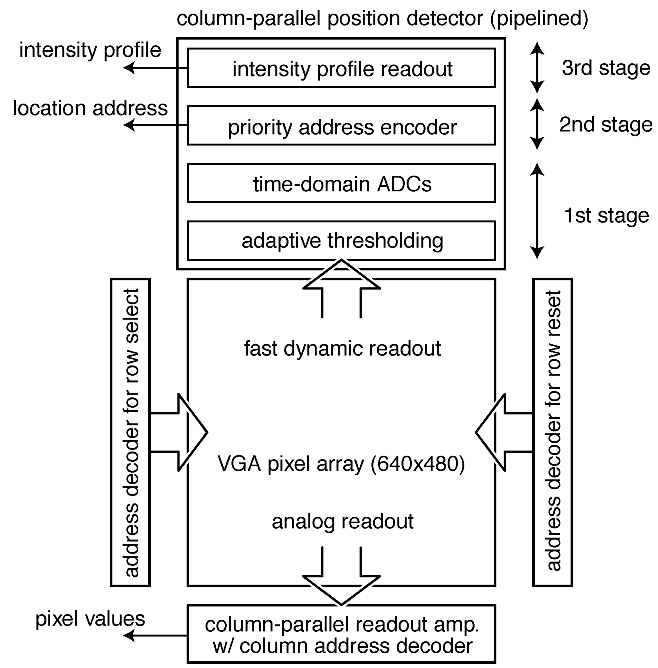

Fig. 3. Block diagram of the sensor.

line is accessed using a high-speed readout scheme, which is realized by a dynamic circuit operation with adaptive thresholding and time-domain approximate ADCs (TDA-ADCs) in 3-D mode [Fig. 2(a)]. Some pixels in a row line, where a strong light incidents, are detected for the location of the projected sheet beam when the pixel value is over the threshold level decided by dark pixel values adaptively [Fig. 2(b)]. The adaptive thresholding is implemented using a slope detector of each column output in time domain to realize quick detection of activated pixels. It is important for the high-speed readout and the quick detection of activated pixels since they require cancellation of a fluctuation of row access speed and robustness in overall scene illuminance. The pixel values over the threshold level are converted to digital by column-parallel TDA-ADCs [Fig. 2(c)]. The results of TDA-ADC contribute to improve sub-pixel accuracy of range finding due to gravity center calculation using intensity profiles of a projected beam. The adaptive thresholding and the approximate ADC are carried out at the same time as dynamic pixel value reading. The results of the adaptive thresholding are transferred to the next pipelined stage to get the left and right edge addresses of the detected pixels [Fig. 2(d)]. In the second stage, a binary-tree priority encoder (PE) provides the location of the activated pixels and also selects the intensity profile of activated pixels for the third pipelined stage. The third stage provides the intensity profile of activated pixels selectively as significant information for high-accuracy range finding [Fig. 2(e)]. In the procedure, the image sensor acquires the location and intensity profiles of a projected sheet beam quickly as requisites for high-accuracy triangulation, and reduces data transmission to achieve high frame rate for real-time and high-resolution range finding.

III. Circuit Configuration and Operation

Fig. 3 shows a block diagram of our proposed 3-D image sensor with a column-parallel position detector for real-time range finding. It consists of a 640 × 480 (VGA) pixel array, address decoders for row select and reset, column-parallel readout amplifiers with a column selector for 2-D imaging, and a column-parallel position detector for 3-D imaging. The sensor has two readout operations: standard analog readout and fast dynamic readout. These readout operations are carried out in a time-division mode for 2-D and 3-D imaging. A column-parallel position detector is composed of three-stage pipelined modules, which are an adaptive threshold circuit, time-domain approximate ADCs, a priority address encoder, and an intensity profile readout circuit. It produces the location address of a projected beam and its intensity profile. In this section, the circuit configuration and operation are described. It achieves the high-speed position detection and the reduction of redundant information for real-time and high-resolution 3-D imaging.

A. Pixel Circuit and High-Speed Readout Scheme

Fig. 4 shows a pixel circuit and the operations of standard analog readout for 2-D imaging and fast dynamic readout for 3-D imaging. In our sensing scheme, a pixel circuit can be the same as a three-transistor CMOS APS [1]. This pixel structure realizes smaller pixel area and higher pixel resolution than the conventional range finders [2]–[4]. In 2-D imaging, N_1 is connected to a supply voltage V_{dd} and N_2 is led to a source follower circuit so that pixels work as the conventional APS. In 3-D imaging, N_1 is precharged to high level before selected and N_2 is connected to the ground level V_{ss}. A bias voltage V_{bn} in Fig. 5 is set to high level in order to connect N_2 to the ground level. After selected, the column output of N_1 begins to decrease depending on each pixel value as shown in Fig. 4. Namely, the

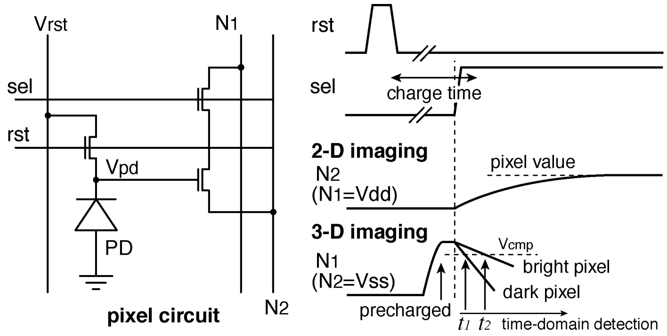

Fig. 4. Pixel circuit configuration and operation.

output N_1 associated with pixels of a stronger incident light is decreasing more slowly so that the time to a threshold voltage is delayed more as well. In the readout method, the relative intensity of each pixels can be acquired shortly after row access, by means of the time-domain dynamic readout scheme with adaptive thresholding. The time-domain approximate ADCs are connected to get the intensity profile.

B. Adaptive Thresholding Circuit

In general, the conventional position sensors detect high-intensity pixels using a predetermined threshold intensity. However, the optimal threshold is influenced by a fluctuation of the row access speed. It also depends on the overall scene illuminance. In our sensing scheme, the threshold intensity $E_{\rm th}$, shown in Fig. 2(b), is decided adaptively by the weakest intensity in each row as shown in Fig. 5(b) and (c). A column output CMP_1 associated with pixels of a weakest incident light is enabled first and it initiates the common trigger signal COM. COM propagates to trigger inputs of column-parallel latch sense amplifiers through delay elements $T_{\rm th}$ and $T_{\rm res}$, which determines a latch timing of the column output CMP_i. DCK_0, which is the delayed signal of COM by $T_{\rm th}$, triggers the first stage of the latch sense amplifiers. The first delay $T_{\rm th}$ keeps a threshold margin $\Delta E_{\rm th}$, shown in Fig. 2(b), from the darkest level in time domain. It cancels a fluctuation of row access speed mainly caused by column-line resistance in order to realizes fast detection with high-speed readout. In addition, it has robustness in overall scene illuminance on some level. The results ACT of the first stage latch indicates whether a pixel is activated or not. They are transferred to the next priority encoder stage.

Fig. 6 shows the relation between the voltage value $V_{\rm pd}$ at photo diode and the discharging time of $V_{\rm col}$ at adaptive thresholding. The voltage level $V_{\rm pd}$ decreases from the provided reset level $V_{\rm rst}$ dependently on the incident light, and then $\Delta V_{\rm pd}$ is converted to the discharging time. The provided reset voltage $V_{\rm rst}$ enables to adjust the adaptive threshold level $\Delta E_{\rm th}$ corresponding to the delay $T_{\rm th}$ as shown in Fig. 6. For example, 200 mV $\Delta V_{\rm pd}$ corresponds to 1.72 and 7.68 ns discharging time when we provide 2.5 and 1.8 V as $V_{\rm rst}$, respectively.

C. Time-Domain Approximate ADC

The intensity of the activated pixels can be acquired by a column-parallel TDA-ADC at the same time of adaptive thresholding. The common trigger signal COM continues to propagate through a delay $T_{\rm res}$ as SA clock signals DCK_n as shown in Fig. 5(c). DCK_n latches the column outputs CMP_i at the nth stage one after another as shown in Fig. 5(b). The arrival timing of a column output depends on the pixel value, so the

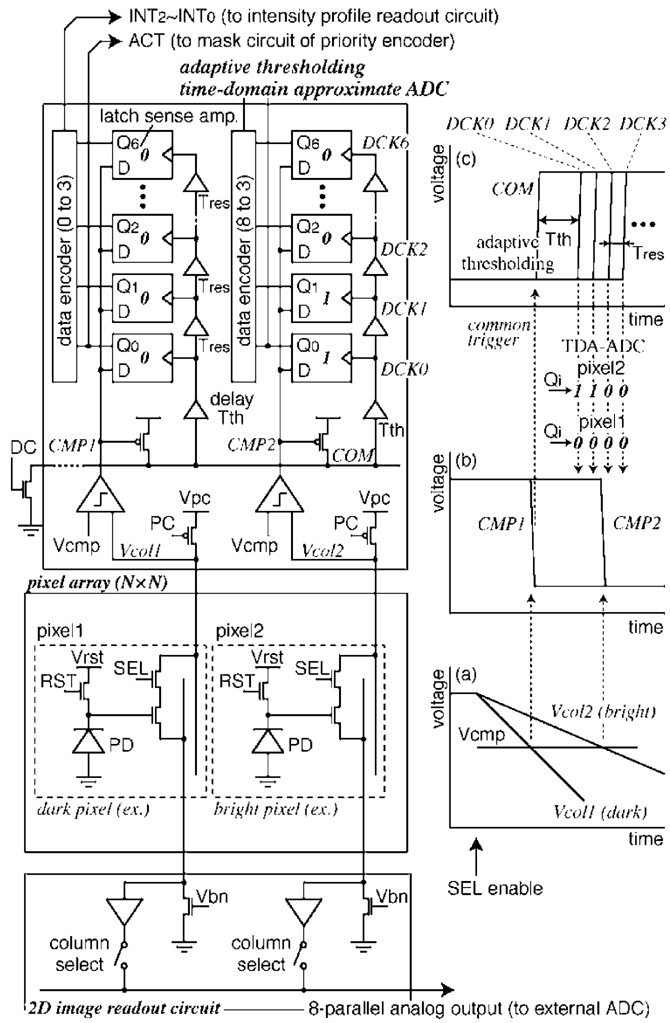

Fig. 5. Schematic and operation of the adaptive thresholding and TDA-ADC.

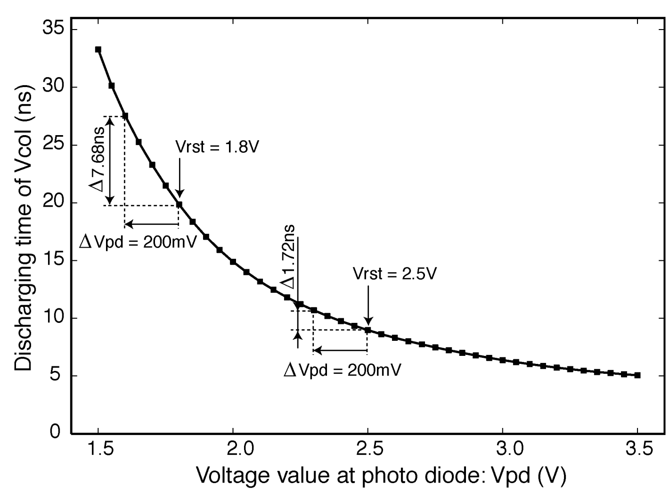

Fig. 6. Relation between pixel value $V_{\rm pd}$ and discharging time of $V_{\rm col}$ at adaptive thresholding.

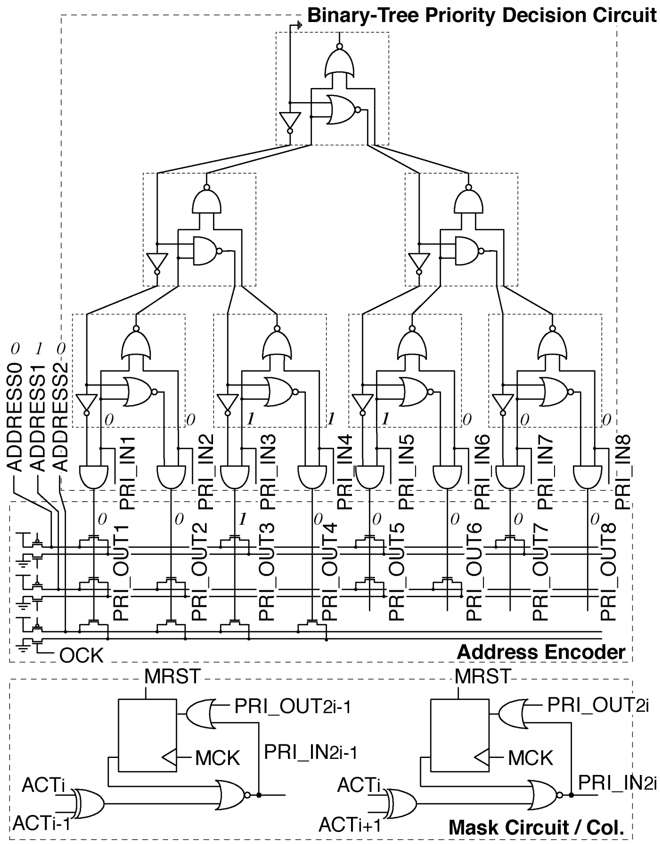

Fig. 7. Schematic of the binary-tree priority encoder.

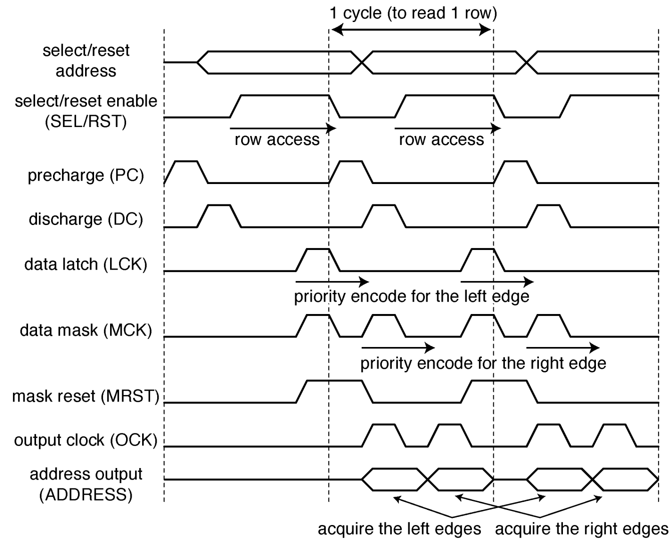

Fig. 8. Timing diagram of the high-speed position detection.

results INT_2–INT_0 of the TDA-ADC show an approximate intensity of each selected pixel normalized by the darkest pixel in the row. For example, in Fig. 5, the common trigger signal COM initiated by the column output CMP_1 of the darkest pixel generates DCK_n in column parallel. The SAs' results of the CMP_1 column are all '0' since the pixel value is below the threshold level. On the other hand, those of the CMP_2 column are '0000011' and the number of '1' represents its intensity ΔE_2 over the threshold level. The number of '1' is encoded in column parallel and transferred to the intensity profile readout circuit, that is, INT_2–INT_0 are '010' as the pixel intensity associated with CMP_2 in Fig. 5. The high-speed readout scheme using the present circuits provides the location of the detected pixels and its intensity profile simultaneously.

D. Column-Parallel Position Detector

Fig. 7 shows a schematic of the binary-tree priority encoder (PE), which receives ACT from the adaptive thresholding circuit. The schematic represents a 16-input PE. Our developed range finder has a 640-input PE for 640 × 480 (VGA) pixel resolution. It consists of a mask circuit, a binary-tree priority decision circuit, and an address encoder. At the mask circuit, ACT_n is compared with the neighbors ACT_{n+1} and ACT_{n-1} to detect the left and right edges using XOR circuits. The priority decision circuit receives PRI_IN_n from the mask circuits and generates the output at the minimum address of activated pixels, for example, PRI_OUT_3 in Fig. 7. The addresses of the left and right edges are encoded at the address encoder. After the first-priority edge has been detected, the edge is masked by PRI_OUT_n and MCK. Then the location of the next priority of activated pixels is encoded. Our improved priority decision circuit keeps high speed in large input number due to a binary-tree structure and a compact circuit cell. Its delay increases in proportion to $\log(N)$, where N is input number.

E. Intensity-Profile Readout Circuit

Using the location of activated pixels from the priority decision circuit, the intensity profile of a projected beam is read out quickly at the intensity profile readout circuit. It is utilized for off-chip gravity center calculation for high sub-pixel accuracy. The intensities of eight activated pixels from the detected left edge are read out using dynamic logics in parallel. The width of a projected sheet beam can be controlled within eight pixels per row. Even if the width is over eight pixels, the center position can be calculated using only the detected left and right edges. A 3-b intensity profile allows a high sub-pixel accuracy under 0.1 pixel theoretically.

Fig. 8 shows its timing diagram. Three-pipelined stages take five clock cycles to detect the location address and intensity profile of activated pixels in each row. A sheet beam scans a target scene using a mirror controlled by a triangular waveform. Then a range map is acquired in one way of the mirror scanning. That is, 30 range_maps/s requires a mirror scanning of 15 Hz. In order to get 640 × 480 range data, 480 row access cycles are carried out 640 times in a mirror scanning on a target scene.

IV. Chip Implementation

We have designed and fabricated a 640 × 480 3-D image sensor using the present architecture and circuits in 0.6-μm CMOS three-metal two-poly-Si process. Fig. 9 shows the chip microphotograph. The sensor has a 640 × 480 pixel array, row select and reset decoders, 2-D image readout circuit, column-parallel TDA-ADCs with adaptive thresholding, a 640-input priority encoder, and an intensity profile readout circuit in 8.9 mm × 8.9 mm die size. It has been designed without on-chip correlation double sampling (CDS) circuits and ADCs for 2-D imaging, but they can be implemented on

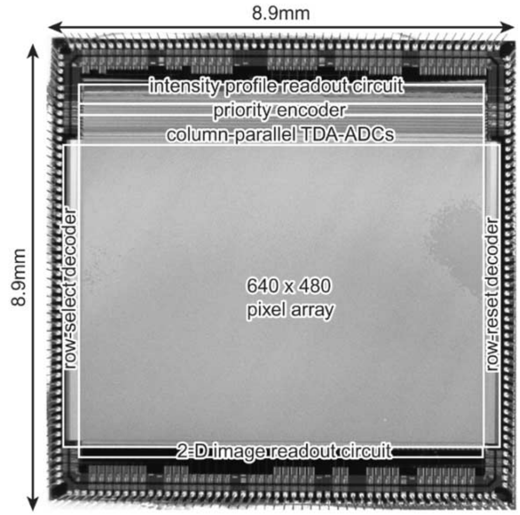

Fig. 9. Chip microphotograph.

TABLE I
SPECIFICATIONS OF THE FABRICATED SENSOR

Process	0.6 μm CMOS 3-metal 2-poly-Si
Die size	8.9 mm × 8.9 mm
# of pixels	640 × 480 pixels (VGA)
# of transistors	1.12M transistors
Pixel size	12.0 μm × 12.0 μm
# of trans. / pixel	3 transistors
Fill factor	29.54 %

the chip the same as other standard CMOS imagers to reduce fixed pattern noise (FPN) and achieve high-speed 2-D imaging. A pixel of the 3-D image sensor has a photo diode and three transistors. Its area is 12 μm × 12 μm with 29.5% fill factor. The photo diode is formed by an n^+-diffusion in a p-substrate. Table I shows the specifications of the fabricated sensor.

V. MEASUREMENT RESULTS

The fabricated range finder has been mounted on a test board in 3-D measurement system based on the light-section method as shown in Fig. 1. In the measurement, the power supply voltage of the image sensor is 5.0 V. The 3-D measurement system is composed of the camera, a laser source of 300 mW (wavelength 665 nm) with a rod lens for beam extension, a scanning mirror with a DAC, an external ADC for 2-D imaging, an FPGA for sensor control, and a PC for display. The photographs of the measurement system are shown in Fig. 10.

A. Frame Rate and Comparison

In 2-D imaging, eight pixel values are readout in parallel, which takes 2 μs. The maximum 2-D imaging speed is 13 fps using 8-parallel high-speed external ADCs. It has a potential of higher speed of 2-D imaging since it is easy to implement the conventional readout techniques, for example, column-parallel ADCs, for fast 2-D imaging in our sensor architecture. In 3-D imaging, the precharge voltage $V_{\rm pc}$ is set to 3.5 V and the compared voltage $V_{\rm cmp}$ at adaptive thresholding is set to 3.0 V. Activated pixels in a row line are accessed and detected within 50 ns at 100-MHz operation. The delay time of the priority encoder

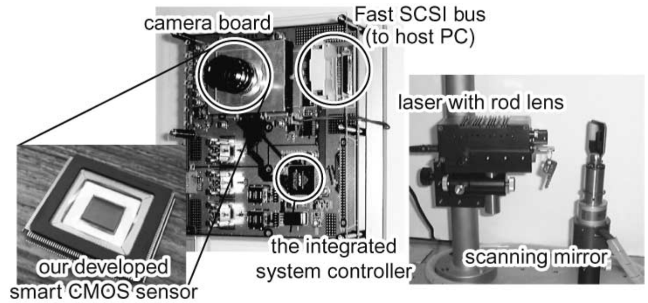

Fig. 10. Photographs of the measurement system.

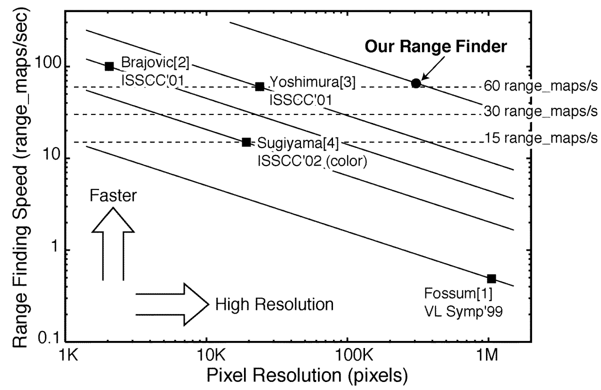

Fig. 11. Range finding speed and pixel resolution with comparison.

stage is 17.2 ns for the left and right edges. The readout time of the intensity profile is 21.5 ns. Their stages are pipelined. Therefore, the location and intensity profile of a projected sheet beam on the sensor plane is acquired in 24.0 μs. The position detection rate for a projected sheet beam is 41.7 k lines/s. Scanning the sheet beam, our 3-D image sensor realizes 65.1 range_maps/s in VGA pixel resolution.

Fig. 11 shows the pixel resolution and 3-D imaging speed of our present image sensor with comparison among the previous designs. A high-speed 2-D imager [1] achieves 1-Mpixel 500-fps 2-D imaging due to column-parallel ADCs, however, it is difficult for their architecture to realize real-time 3-D imaging independently of its pixel resolution if it is applied to a range finding system based on the light-section method. State-of-the-art range finders [2]–[4] achieve $>$15 range_maps/s in each pixel resolution. Their pixel/peripheral circuits are too large to realize over-VGA resolution and their architectures are intolerant to keep real-time 3-D imaging rate in high pixel resolution as shown in Fig. 11. Our 3-D image sensor is the first real-time range finder with the capability of VGA resolution based on the light-section method.

B. Range Accuracy

Fig. 12 shows measured distances of a white flat board at 30 range_maps/s operation by the present range finder. Here, the baseline, which is a distance between a camera and a beam source, is 431.5 mm. The view angle of the camera is 30°. A target object is placed at a distance of around 1200 mm from the camera. Our 3-D imager can acquire the intensity profile of a projected sheet beam to achieve high sub-pixel accuracy for precise range finding. The standard deviation of measured error

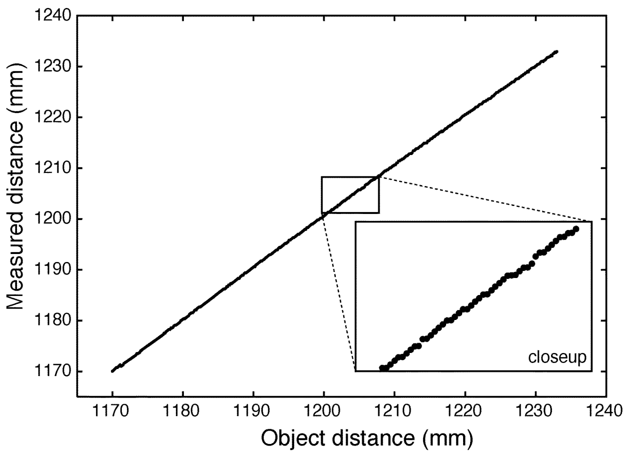

Fig. 12. Measured range accuracy.

TABLE II
PERFORMANCE OF THE PRESENT 3-D IMAGER

Power supply voltage	5.0 V
Power dissipation	305 mW (@ 10 MHz)
Max. 2-D imaging rate	†13.0 frames/sec
Max. position detection rate	41.7k lines/sec
Max. range finding rate	65.1 range_maps/sec
Range accuracy (max. error)	0.87 mm (@ 1200 mm)

†limited by off-chip ADC

is 0.26 mm and the maximum error is 0.87 mm at a distance of 1170–1230 mm by gravity center calculation using acquired intensity profiles. For comparison, the standard deviation of measured error is 0.54 mm and the maximum error is 2.13 mm by the conventional binary-based position calculation. That is, our 3-D image sensor achieves less error than half of the conventional methods based on a binary image. An intensity profile could be distorted by device fluctuation, but the measurement results show that it is effective to get the approximate intensity profile of activated pixels. The sensor performances are summarized in Table II.

C. Measured Images

Our 3-D image sensor can acquire both 2-D images and 3-D images in time division. Fig. 13 shows measured images by the present 3-D image sensor. Fig. 13(a) is a captured VGA 2-D image of a hand. Fig. 13(b)–(d) show its range maps displayed from different view angles. The brightness of the range maps represents the distance from the range finder to the target object. The range data has been already plotted in 3-D space, so it can be rotated freely as shown in Fig. 13(b)–(d). Fig. 13(e) is a wire frame reproduced by the measured range data and Fig. 13(f) is a close-up of Fig. 13(e). The measured images show that our real-time 3-D image sensor with VGA pixel resolution realizes high spatial and high range resolution 3-D imaging.

The image sensor has a possibility of detection failure on a black or complementary red part of a target object since the reflected intensity of a projected beam degrades. A long exposure avoids the detection failure with the voltage control of $V_{\rm rst}$ and $V_{\rm cmp}$ on the condition that the reflected beam is still stronger than the high contrast scene. Therefore, the projected beam intensity also limits the range finding speed in proportion. The current 3-D imaging system requires a strong beam intensity of 300 mW in a room with a constant ambient light to achieve the maximum range finding speed. In the future, it can be improved by a high-sensitivity photo diode with a micro lens, a correlation technique to suppress an ambient light, and so on.

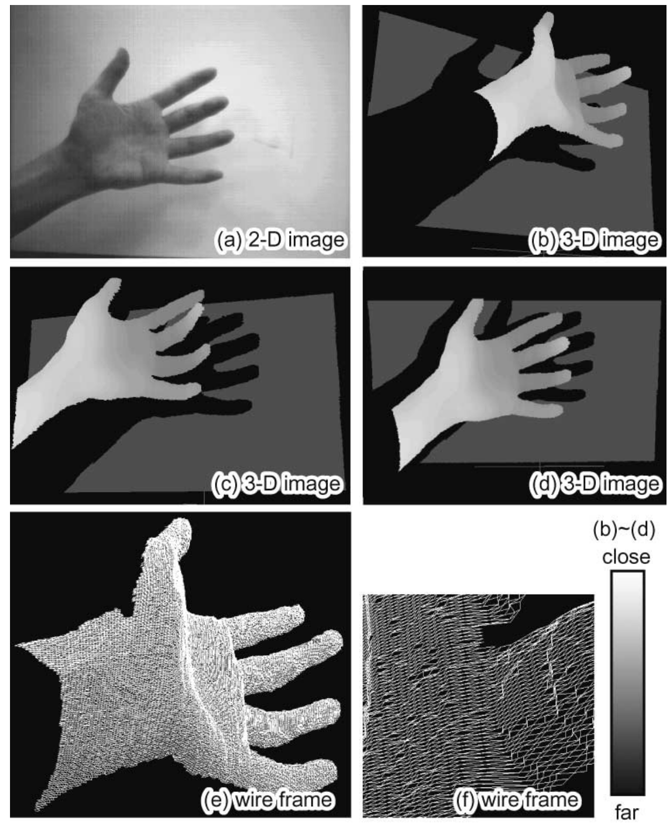

Fig. 13. Measurement results of the present sensor.

In a 3-D measurement system based on triangulation, the whole range data of a target object cannot be obtained because of a dead angle of a camera and a beam projector. Therefore, the acquired 3-D image lacks range data of the side and back face. A 3-D measurement system using a couple of cameras and projectors realizes all-direction 3-D imaging.

VI. Conclusion

A 640 × 480 real-time 3-D image sensor using a high-speed readout scheme and a column-parallel position detector has been presented. It is the first 3-D image sensor based on the light-section method to realize VGA pixel resolution and real-time range finding. Our high-speed readout scheme realizes the use of a standard and compact pixel circuit to get the location and intensity profile of a projected sheet beam on the sensor plane quickly. The column-parallel position detector suppresses redundant data transmission for a real-time measurement system. The maximum range finding speed is 65.1 range_maps/s. The maximum range error is 0.87 mm and the standard deviation of error is 0.26 mm at 1200-mm distance due to an intensity profile. A 2-D image and a high-resolution 3-D image have been acquired by the 3-D measurement system using the present image sensor.

ACKNOWLEDGMENT

The sensor in this study has been designed with CAD tools of Synopsys Inc. and Cadence Design Systems Inc., and fabricated through the VLSI Design and Education Center (VDEC), University of Tokyo, in collaboration with Rohm Corp. and Toppan Printing Corp.

REFERENCES

[1] A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E. R. Fossum, "A high speed, 500 frames/s, 1024 × 1024 CMOS active pixel sensor," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 1999, pp. 137–138.

[2] V. Brajovic, K. Mori, and N. Jankovic, "100 frames/s CMOS range image sensor," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2001, pp. 256–257.

[3] S. Yoshimura, T. Sugiyama, K. Yonemoto, and K. Ueda, "A 48 k frame/s CMOS image sensor for real-time 3-D sensing and motion detection," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2001, pp. 94–95.

[4] T. Sugiyama, S. Yoshimura, R. Suzuki, and H. Sumi, "A 1/4-inch QVGA color imaging and 3-D sensing CMOS sensor with analog frame memory," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2002, pp. 434–435.

[5] Y. Oike, M. Ikeda, and K. Asada, "Smart sensor architecture for real-time and high-resolution range finding," in *Proc. Eur. Solid-State Circuit Conf. (ESSCIRC)*, 2002, pp. 105–108.

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