A CMOS Image Sensor for High-Speed Active Range Finding Using Column-Parallel Time-Domain ADC and Position Encoder

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***Abstract*—In this paper, a smart image sensor for real-time and high-resolution three-dimensional (3-D) measurement to be used for sheet light projection is presented. It realizes not only a sufficiently high frame rate for real-time 3-D measurement, but also high pixel resolution due to a small pixel circuit and high subpixel accuracy due to gravity center calculation using an intensity profile. Simulation results show that the ultimate frame rate is 32.6 k frames/s (i.e., 31.8 range_map/s) in a 1024 × 1024 pixel sensor. A 3-b intensity profile allows subpixel accuracy under 0.1 pixel. The sensor using this architecture can acquire a two-dimensional (2-D) image as well, so a texture-mapped 3-D image can be reproduced by the same sensor. A 128 × 128 smart image sensor has been developed and successfully tested. A 2-D image, a range map, and a texture-mapped 3-D image have been acquired by the 3-D measurement system using the fabricated sensor.**

***Index Terms*—High resolution, position encoder, priority encoder, range finding, real time, smart image sensor, time-domain analog-to-digital (ADC).**

I. Introduction

In RECENT years, we have often seen three-dimensional (3-D) computer graphics in movies and televisions and have handled them interactively using personal computers and video game machines. A real-time range-finding system provides new attractive applications. The triangulation-based 3-D measurement using sheet light projection allows high-accuracy range-finding by simple calculation. It, however, requires thousands of images every second for real-time 3-D measurement. For example, a 1024×1024 range map in video rate requires 30 k frames/s. It is difficult to realize real-time 3-D measurement by a standard readout architecture such as CCD. Even the high-speed CMOS active pixel sensor (APS) using column-parallel analog-to-digital converters (ADCs) [1] realizes 500 fps at most.

Some position sensors for the fast range-finding are reported in [2], [3]. The sensor using pixel-parallel architecture [2] can acquire a 192×124 range map in video rate (i.e., 30 range_map/s). However, it has a large circuit for a frame memory and an ADC in pixel and it is difficult to realize high-pixel resolution. The sensor using a row-parallel winner-take-all (WTA) circuit [3] can acquire a 64×64 range map in 100 range_map/s. Its pixel size can be smaller than that in [2] due to the row-parallel architecture. The pixel resolution, however, is limited by the precision of a current-mode WTA circuit. It is also difficult to realize a sufficiently high frame rate for real-time range finding with high pixel resolution.

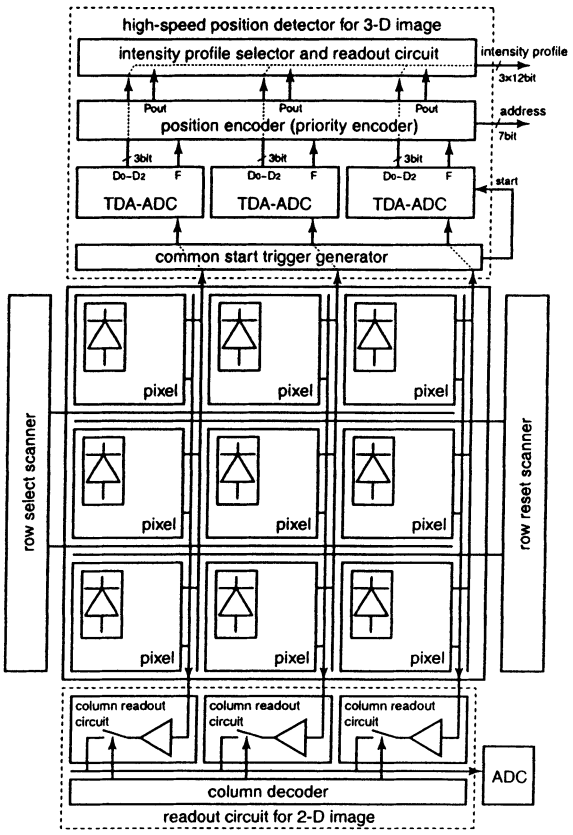

Fig. 1. Block diagram of the sensor architecture.

In this paper, a smart image sensor for real-time high-resolution range finding is proposed to be used for sheet light projection. The architecture can realize not only sufficient high-speed position detection of the projected sheet light for real-time 3-D measurement, but also high pixel resolution due to a three-transistor (3T) pixel circuit. The present sensor can acquire both the position and the intensity profile of the projected light simultaneously. The intensity profile is used for higher accuracy range finding by gravity center calculation than the conventional smart position sensors [2]–[6]. In addition, the sensor can acquire a two-dimensional (2-D) image as well, so a texture-mapped 3-D image can be reproduced by the same sensor. A 128×128 smart image sensor has been developed and successfully tested.

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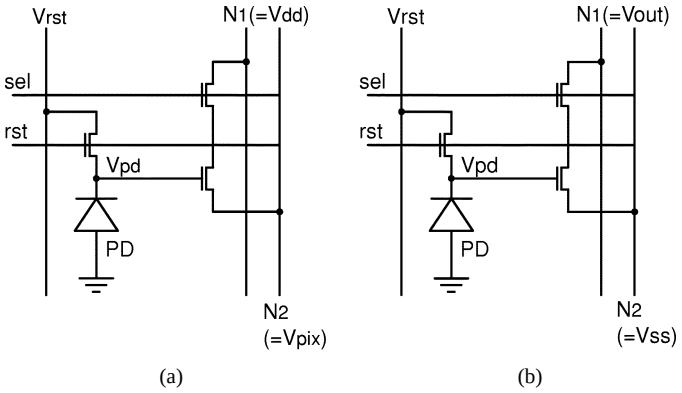

Fig. 2. Pixel configurations: (a) 2-D mode. (b) 3-D mode.

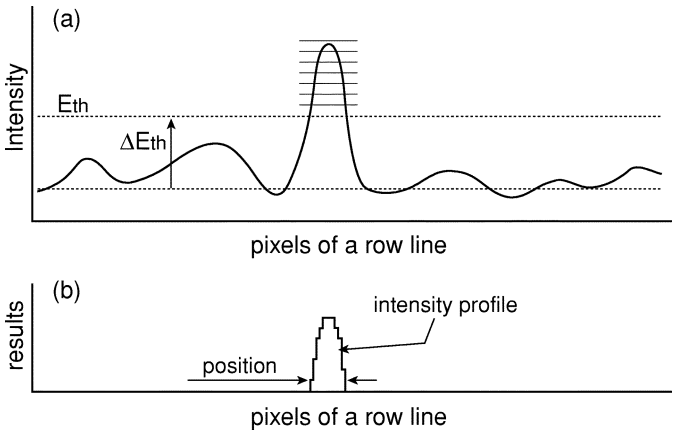

Fig. 3. Pixel intensities and results of the TDA-ADC: (a) pixel intensities and (b) its results.

II. Sensor Architecture

Fig. 1 shows a block diagram of the proposed sensor architecture. The sensor has a high-speed position detector for 3-D measurement, a pixel array, row —select and reset scanners, and a readout circuit for 2-D images. The high-speed position detector consists of three pipelined modules as follows: time-domain approximate ADCs (TDA-ADCs) with a common trigger generator, a priority encoder composed of a priority decision circuit and an address encoder, and an intensity profile readout circuit. The readout circuit for a 2-D image consists of column-parallel source-follower buffers, a multiplexer with a column selector, and an ADC.

A. Pixel Circuit

In the present architecture, a pixel circuit can be the same as the 3T CMOS APS [7]. This pixel structure realizes a small pixel area and high pixel resolution in general. The pixel circuit in the architecture has two operation modes as follows.

1) In 2-D mode, the node N_1 is fixed to the supply voltage V_{dd}, and the node N_2 leads to the readout source follower circuit as shown in Fig. 2(a).
2) In 3-D mode, the node N_1 is the output of the dynamic circuit, and the node N_2 is connected to the ground V_{ss} as shown in Fig. 2(b). After the node N_1 is charged to a precharge voltage V_{pc} and the pixel is selected, the output voltage $V_{\rm out}$ at N_1 begins to decrease depending on the pixel value V_{pd}. The pixel values are detected as discharging times. Namely N_1 associated with pixels of a strong incident light is decreasing more slowly.

B. TDA-ADC

In the present architecture, the pixels of a strong incident light are quickly detected by TDA-ADCs. In general, a position sensor detects the pixels of stronger intensity than the fixed threshold intensity. In the TDA-ADC, the threshold intensity $E_{\rm th}$ can be decided adaptively by the weak intensity in each row, as shown in Fig. 3(a). In addition, both the position and the intensity profile of the projected light can be acquired as shown in Fig. 3(b). The intensity profile allows high subpixel accuracy by gravity center calculation.

Fig. 4 shows the structure of the TDA-ADC. It consists of a precharge circuit, an amplifier, a common trigger generator, delay circuits, latched sense amplifiers (SAs) for a timing memory, and a pixel value encoder. The TDA-ADC employs the speed of decreasing voltages at the output lines CO_n for a threshold logic and an approximate analog-to-digital conversion. The stronger the incident light at the pixel is, the slower the output voltage of CO_n decreases.

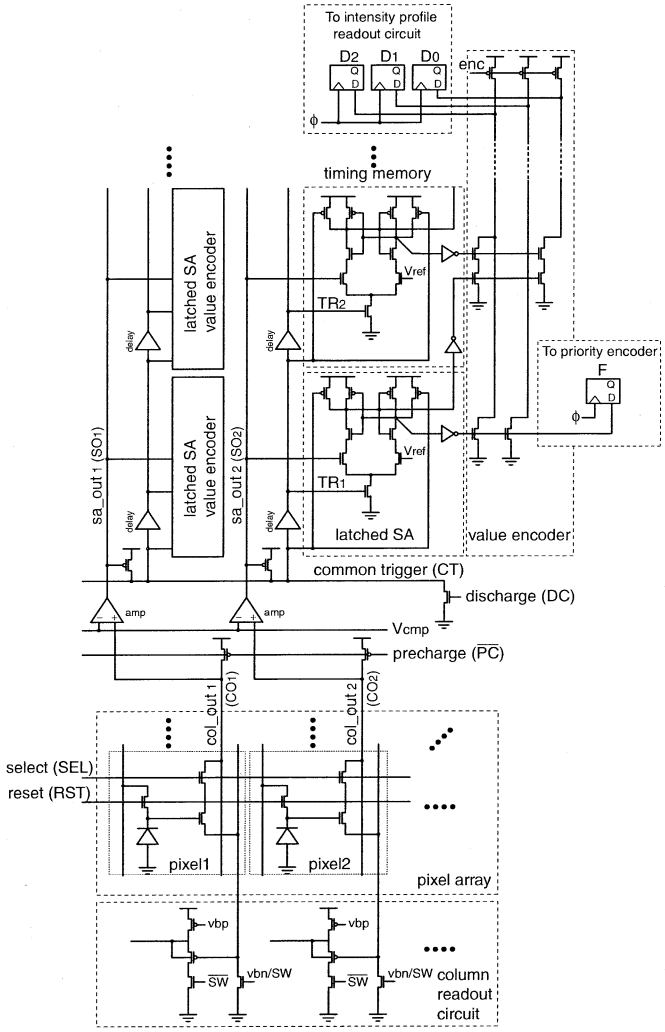

Fig. 4. Structure of the TDA-ADC.

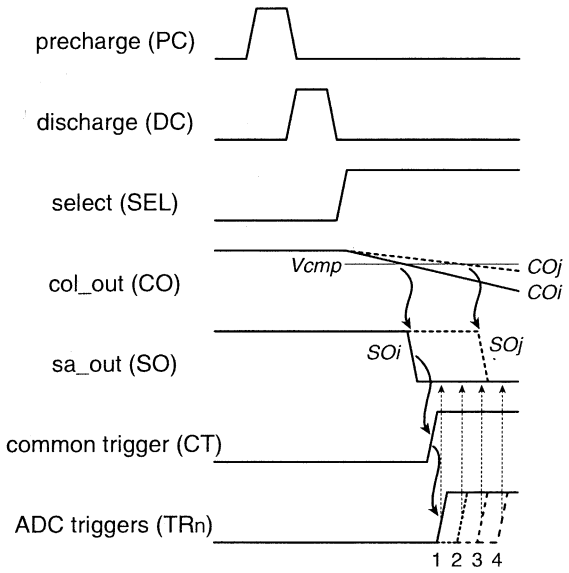

Fig. 5. Timing diagram of the TDA-ADC.

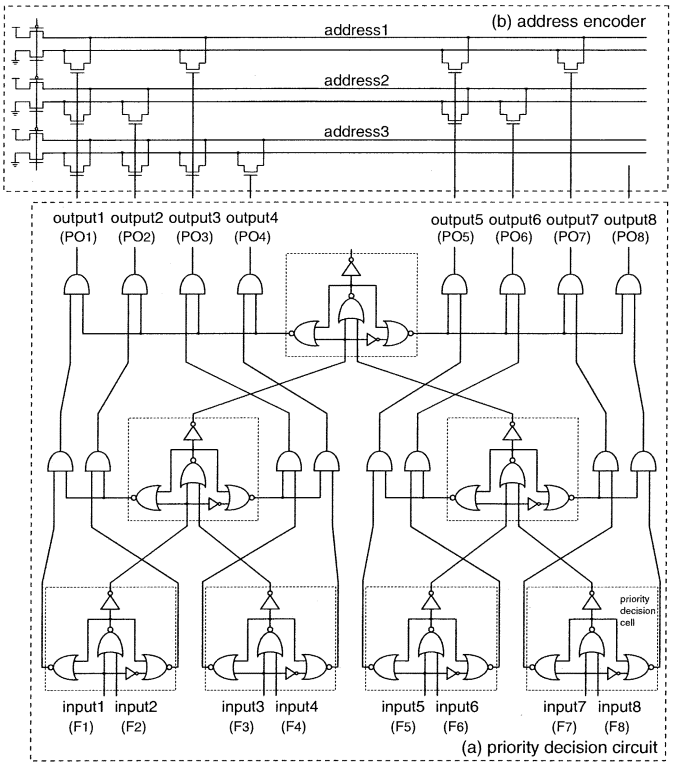

Fig. 6. Schematic of the priority decision circuit.

Fig. 5 shows a timing diagram of the TDA-ADC. The output voltages of each column CO_n are precharged to V_{pc} by the signal *PC*. The common trigger line *CT* is then discharged by the signal *DC*. Pixels of a row line are selected by *SEL* and the output voltages at CO_n begin to decrease according to each pixel value. SO_n is thrown OFF when the voltage at CO_n is below the reference voltage V_{cmp}. The common trigger line *CT* is thrown ON by the first-arrival signal of SO_n, that is, the trigger is initiated by the weakest intensity. *CT* propagates through delay circuits, so that the trigger signals TR_n for the latched SAs are thrown ON one after another. The latched SAs

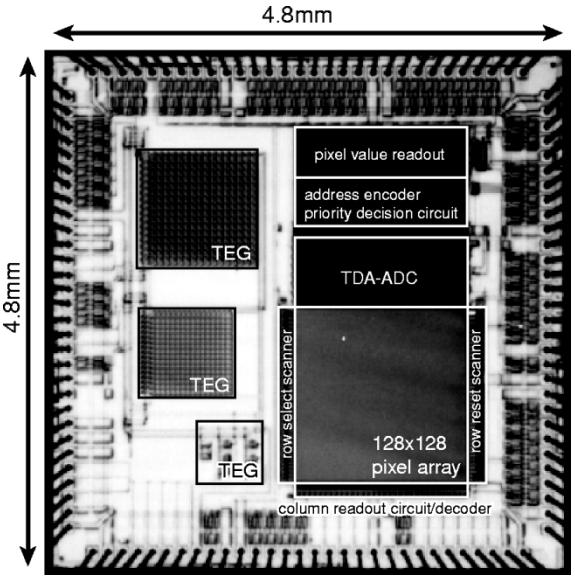

Fig. 7. Microphotograph of the fabricated sensor.

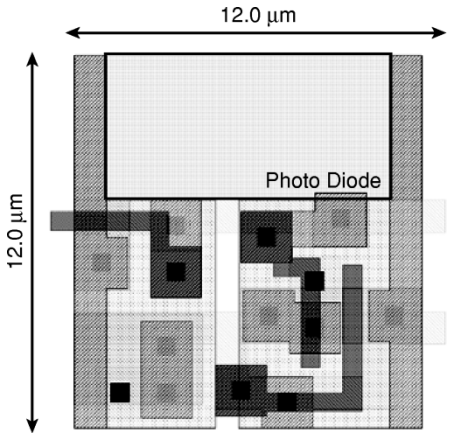

Fig. 8. Layout of the pixel circuit.

sample and hold SO_n in each timing with TR_n. For example, the signal SO_j in Fig. 5 changes between TR_3 and TR_4, so the latched sense amplifiers of $n \geq 4$ are thrown OFF. The intensity values of detected pixels in a timing memory are encoded and transferred to an intensity-profile readout circuit. The result of the first latched SA is transferred to a priority encoder for position detection.

The TDA-ADC can provide the locations of the detected pixels and its intensity profile. The threshold intensity is decided by the delay time between the first arrival SO_n and the first trigger TR_1, so the TDA-ADC can keep the threshold gain ΔE_{th} from the background intensity. It can adapt to the delay fluctuations of each row caused by the column line resistance. The resolution of intensity profile corresponds to one delay interval of TR_n.

C. Priority Encoder

The present architecture has a priority encoder to search the position of the detected pixels and to encode its address quickly. The priority encoder consists of a priority decision circuit and an address encoder as shown in Fig. 6. The priority decision

TABLE I
PARAMETERS OF THE FABRICATED SENSOR

Process	0.6 μm CMOS 3-metal 2-poly-Si
Chip size	4.8 mm × 4.8 mm
Sensor size	3.32 mm × 1.88 mm
Array size	128 × 128 pixels
Pixel size	12.0 μm × 12.0 μm
# trans. / pixel	3 transistors
Fill factor	29.54 %

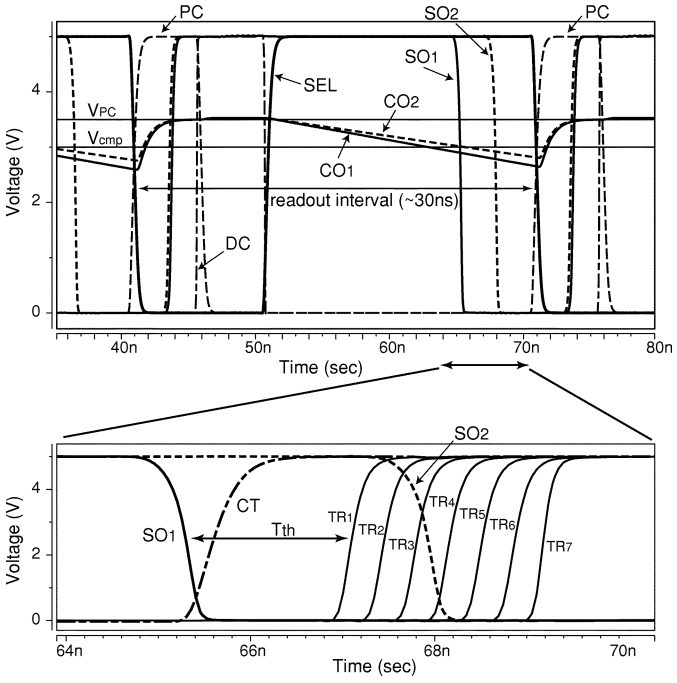

Fig. 9. Simulated wave forms.

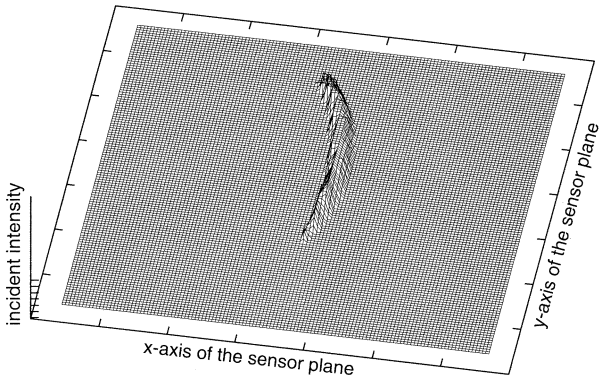

Fig. 10. Measured intensity profile of the projected light on a sphere-shaped object.

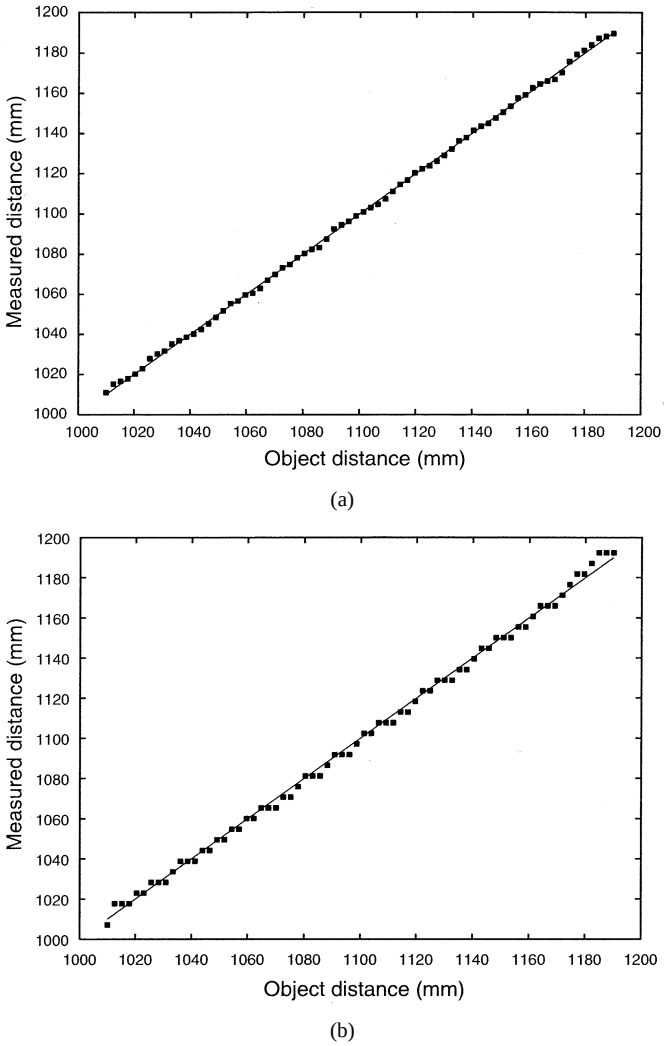

Fig. 11. Linearity of measured range data. (a) Using position and intensity profile. (b) Using position only.

circuit can detect only a prior active input (i.e., the left edge of the detected pixels), and the output corresponding to the prior active input is thrown ON. Its address is encoded and outputted by the address encoder as shown in Fig. 6(b). After encoding, the prior active input can be masked by the output of the priority decision circuit sequentially in order to acquire the address of the next peak of intensity.

D. Intensity-Profile Readout Circuit

After address encoding of the detected pixels, the intensities of them are read out in order to acquire the intensity profile of the peak. The input signals of an intensity-profile readout circuit are 3-b intensities from TDA-ADCs and the result of the priority decision circuit. The intensities of 12 activated pixels from the detected left edge are read out using dynamic logics in parallel. The width of a projected sheet beam can be controlled within 12 pixels per row. Even if the width is over 12 pixels, the center position can be calculated using only the detected left and right edges. A 3-b intensity profile allows a high subpixel accuracy under 0.1 pixel theoretically. In general, the position detection using a binary image realizes no more than 0.5-pixel accuracy. The accuracy of measured range data is improved proportionally to the subpixel accuracy.

TABLE II
PERFORMANCE COMPARISON

	the present sensor	the conventional smart position sensors		the standard CMOS APS
		[2]	[3]	[1]
process	0.6 μm CMOS process	0.35 μm CMOS process	—	0.5 μm CMOS process
trans./pix.	3	35 + 2 cap.	> 9	3
pixel size	12.0×12.0 μm^2	46.4×54.0 μm^2	—	10.0×10.0 μm^2
fill factor	29.54 %	25 %	—	45%
array size	128 × 128	192 × 124	64 × 32	1024 × 1024
max. fps	260k	48k	—	500 (full 2-D image)
range_map/sec*	2034	30 (at 12k fps)	100	0.5
sub-pix accuracy	< 0.1 pixel (3bit)	depends on fps	0.5 pixel (1bit)	(10bit)

* # range data is considered to be the same resolution as # pixels

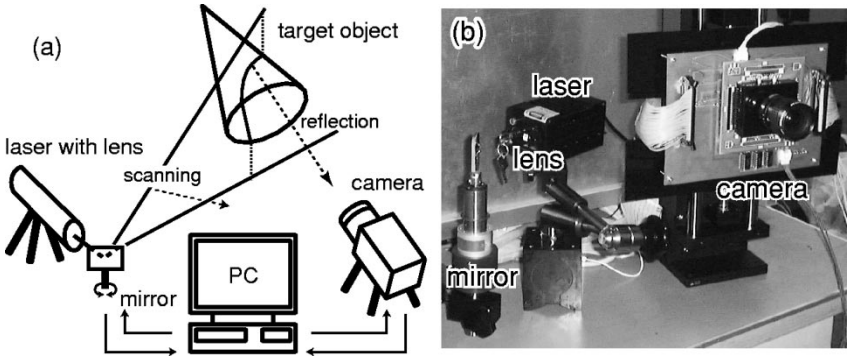

Fig. 12. Three-dimensional measurement system: (a) composition and (b) photograph.

III. CHIP IMPLEMENTATION

We designed and fabricated a smart image sensor using the present architecture in 0.6-μm CMOS process.[1] Fig. 7 shows a microphotograph of the fabricated smart image sensor. The sensor has a 128 × 128 pixel array, 3-b TDA-ADCs, a 128-input priority encoder, a 3 × 12-b parallel intensity-profile readout circuit, select and reset scanners, and a column-parallel readout circuit. In 2-D mode, a multiplexer outputs four pixel values each, and the pixel values are converted to digital by external ADCs. The prototype has been designed without on-chip correlation double sampling (CDS) circuits, but a CDS circuit can be implemented on the chip the same as other standard CMOS imagers to reduce fixed pattern noise (FPN). Fig. 8 shows a mask layout of a pixel. The pixel has a photodiode and three transistors, and its area is 12 μm × 12 μm with a 29.5% fill factor. The photodiode is formed by an n^+-diffusion in a p-substrate. Table I shows the parameters of the fabricated sensor.

[1]The sensor in this study has been designed with CAD tools of Avant! Corporation and Cadence Design Systems Inc., and fabricated through VLSI Design and Education Center (VDEC), University of Tokyo, in collaboration with Rohm Corporation and Toppan Printing Corporation.

IV. PERFORMANCE EVALUATION

A. Frame Rate

Fig. 9 shows the simulated wave forms of the TDA-ADC. After a row line is selected by *SEL*, the output CO_1 and CO_2, which are precharged to V_{pc}, begin to decrease. In this simulation, the pixel values are 2.4 and 2.2 V. The present sensor can read one row line in 30 ns. The delay time of the priority encoder is 7.2 ns, and the readout time of the intensity profile is 4.3 ns. The ultimate frame rate of the sensor is 260 k frames/s (i.e., 2034 range_map/s). The present architecture is capable of acquiring a 1024 × 1024 range map in 31.8 range_map/s.

B. Subpixel Accuracy

Fig. 10 shows an intensity profile of the projected sheet light on a sphere-shaped target object. The position of the projected light is calculated by gravity center calculation using the intensity profile. Fig. 11 shows measured distances using (a) the positions and the intensity profile and (b) the positions only. The standard deviation of measured error is 1.18 mm and the maximum error is 2.64 mm at a distance of 1000–1200 mm by gravity center calculation using an intensity profile. On the other hand, the standard deviation is 2.58 mm and the maximum error

is 7.61 mm without an intensity profile. An intensity profile could be distorted by device fluctuation, but the measurement results show that the present sensor can realize higher accuracy than the conventional position sensor using a binary image.

C. Comparison

Table II shows a performance comparison among the present sensor, the conventional smart position sensors [2], [3], and the standard CMOS APS [1]. The present sensor allows high integration almost the same as that in [1] due to a smaller pixel circuit than the other smart position sensors [2], [3]. For example, a 1024×1024 sensor using our architecture occupies 14.8 mm $\times$ 12.8 mm in 0.6-μm CMOS process. Its size is practical for fabrication. In addition, it has a sufficiently high frame rate for real-time 3-D measurement with high pixel resolution. With regard to subpixel accuracy, the present sensor can realize higher accuracy without loss in frame rate. The present architecture has advantages of real-time and high-resolution range finding.

V. Application to 3-D Measurement

Fig. 12(a) illustrates the measurement system based on triangulation using the present smart image sensor. The 3-D measurement system is composed of the camera using the fabricated sensor, a laser (wavelength 665 nm) with a rod lens for beam extension, a scanning mirror, and a PC with a digital I/O board and ADC/DAC boards. The PC employs a digital I/O board for the sensor control, an ADC board for acquiring pixel values in 2-D mode, and a DAC board for the scanning mirror control. Fig. 12(b) shows a photograph of the measurement system.

A 3-D range map can be calculated from the positions of the projected laser beam on the sensor plane and both positions of the sensor and the projected light source. In the measurement, the camera acquires 128 frames during one scan of the projected laser beam. Fig. 13(a) shows an acquired 2-D image by the present sensor. Fig. 13(b) shows the range data calculated and calibrated by the measurement results in 3-D mode. The range data are plotted at a horizontal angle of 45°. The present sensor can acquire both a 2-D image and a range map, and a texture-mapped 3-D image can be reproduced as shown in Fig. 13(c). A 3-D image can be observed not only at an angle of 0°, but also at a free angle.

In a 3-D measurement system based on triangulation, the whole range data of a target object cannot be obtained because of a dead angle of a camera and a laser projector. Also, the range data close to the border is inaccurate in general. Therefore, the acquired 3-D image lacks range data of the side view. A 3-D measurement system using a couple of cameras and projectors can acquire an all-direction 3-D image.

VI. Conclusion

A smart image sensor for real-time and high-resolution range finding has been proposed. It realizes not only enough high frame rate for real-time 3-D measurement, but also high pixel resolution due to a small pixel circuit and high subpixel accuracy due to gravity center calculation using an intensity profile. The present sensor can acquire a 2-D image as well, so a texture-mapped 3-D image can be reproduced by the same sensor. A 128×128 smart image sensor has been developed and successfully tested. The ultimate frame rate is 260 k frames/s (i.e., 2034 range_map/s) in a 128×128 pixel array. The standard deviation of measured error is 1.18 mm and the maximum error is 2.64 mm at a distance of 1000–1200 mm. A 2-D image, a range map, and a texture-mapped 3-D image have been acquired by the 3-D measurement system using the fabricated sensor.

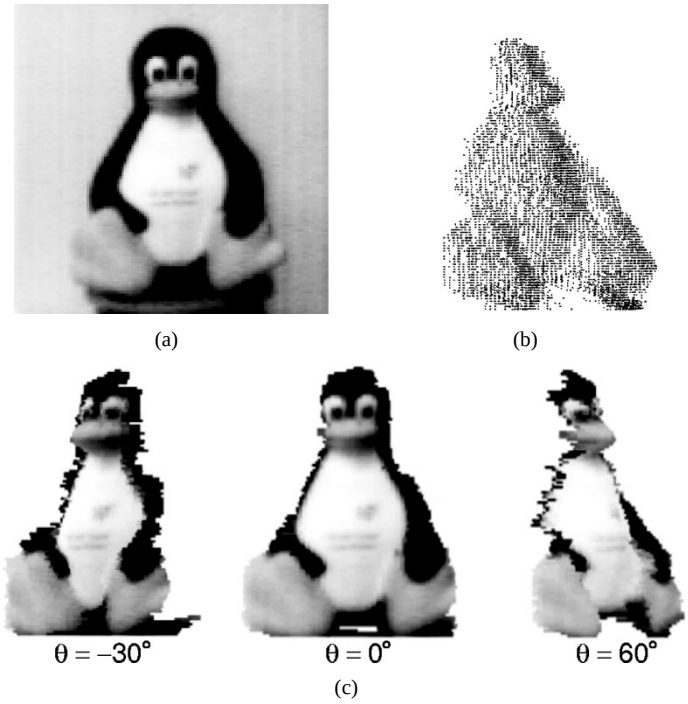

Fig. 13. Acquired and reproduced images. (a) Acquired 2-D image by the present sensor. (b) Acquired range data by the present sensor. (c) Reproduced 3-D images.

References

[1] A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E. R. Fossum, "A high speed, 500 frames/s 1024×1024 CMOS active pixel sensor," in *VLSI Circuits Tech. Dig.*, 1999, pp. 137–138.

[2] S. Yoshimura, T. Sugiyama, K. Yonemoto, and K. Ueda, "A 48 kframe/s CMOS image sensor for real-time 3-D sensing and motin detection," in *ISSCC Tech. Dig.*, 2001, pp. 94–95.

[3] V. Brajovic, K. Mori, and N. Jankovic, "100 frames/s CMOS range image sensor," in *ISSCC Tech. Dig.*, 2001, pp. 256–257.

[4] A. Makynen *et al.*, "A binary photodetector array for position sensing," *Sens. Actuators A, Phys.*, vol. 65, pp. 45–53, 1998.

[5] M. de Bakker, P. W. Verbeek, E. Nieuwkoop, and G. K. Steenvoorden, "A smart range image sensor," in *Proc. Eur. Solid-State Circuits Conf.*, 1998, pp. 208–211.

[6] T. Nezuka, M. Hoshino, M. Ikeda, and K. Asada, "A smart image sensor with novel implementation of quad-tree scan," in *Proc. Eur. Solid-State Circuits Conf.*, 2000, pp. 412–415.

[7] E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip," *IEEE Trans. Electron Devices*, vol. 44, pp. 1689–1698, Oct. 1997.

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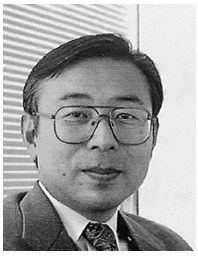

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In 1980, he joined the Faculty of Engineering, University of Tokyo, and became a Lecturer, an Associate Professor, and a Professor in 1981, 1985, and 1995, respectively. From 1985 to 1986, he was with Edinburgh University, Edinburgh, U.K., as a Visiting Scholar supported by the British Council. From 1990 to 1992, he served as the first Editor of English version of the *IEICE Transactions on Electronics*. In 1996, he established VDEC (VLSI Design and Education Center) with his colleagues at the University of Tokyo. It is a center supported by the government to promote education and research of VLSI design in all the universities and colleges in Japan. He is currently in charge and the head of VDEC. His research interest is design and evaluation of integrated systems and component devices. He has published more than 390 technical papers in journals and conference proceedings.

Prof. Asada has received best paper awards from the Institute of Electrical Engineers of Japan (IEEJ), the IEICE, and ICMTS1998/IEEE. He is a member of the IEICE and the IEEJ. He is currently Chair of the IEEE/SSCS Japan Chapter.